Technical Manual

Commodore PC 40

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1. Introduction

The main board is a high performance 16-bit system board, which is hardware compatible with the IBM PC/AT. The standard operating system is MS-DOS version 3.x. Multi-user and multi-tasking functions are supported under the UNIX operating system.

2. Features

- 80286 (10 MHz) microprocessor to support memory-management and virtual memory functions.
- 16 megabytes physical memory range (24-bit address bus).
- ROM-based automatic power-on self-test of system components.
- 1 MB on-board DRAM

  Eight I/O expansion slots for 8-bit and 16-bit peripherals.
- Seven DMA channels.
- Three programmable timers.
- 15 interrupt levels

- System clock/calendar system configuration, CMOS RAM and battery back-up. (Motorola MC 146818).

- Bi-directional keyboard interface.

- Buzzer for sound system and LED for power-on indication.

- Socket for the 80287 mathematical co-processor.

Main board input current:

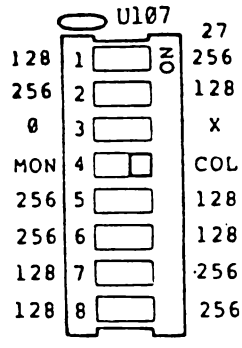
Voltage	Ampere
+ 5V	7A
- 5V	0A
+12V	0A
-12V	0A

2.2 DIP switch setting

There is only one eight-position DIP switch block on the system board, located on the left side near to the expansion slots. The DIP switch is called U107.

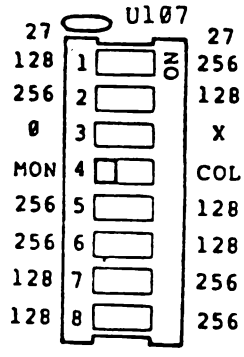
DIP switch setting for display monitor type:

a) if you use color video monitor, flip the DIP switch 4 to the side marked COL(for colour).



picture 1

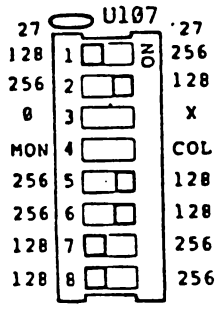
b) If you use monochrome video monitor, flip the DIP switch to the side marked MON (for monochrome).



Picture 2

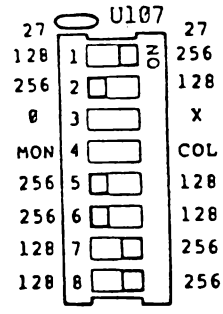
DIP switch setting for memory chip type:

a) If you use the 27128, tip the DIP switches to the side marked with 128.



Picture 3

b) If you use the 27256, tip the DIP switches to the side marked with 256.



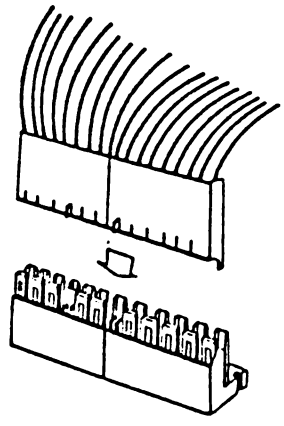
Picture 4

2.2 Power connector

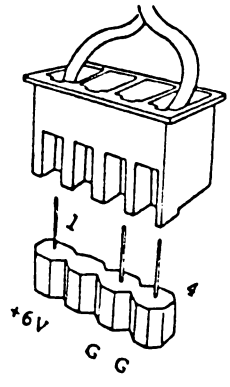
On the main board, near the upper right corner, there are two power supply connectors. The on-board location is labeled J3. The pin functions are:

Pin No.	Description
1	Power good
2	+ 5V
3	+12V
4	-12V
5	GND
6	GND
7	GND
8	GND
9	- 5V
10	+ 5V
11	+ 5V
12	+ 5V

Connect two of the connectors from the power supply into the main board as shown in the following figure. When plugging, be careful of their orientation. Each power connector is keyed to avoid mismatching. If the plug does not go in easily, turn it over and retry, or try plugging it into another.



Picture 5



Picture 6

2.3 Battery and Jumper J2

The battery connector is located on J4. (See Picture 6). The pin functions are as given below:

Pin No.	Description
1	+ 6V
2	not connected
3	GND
4	GND

Jumper J2 (pin-out)

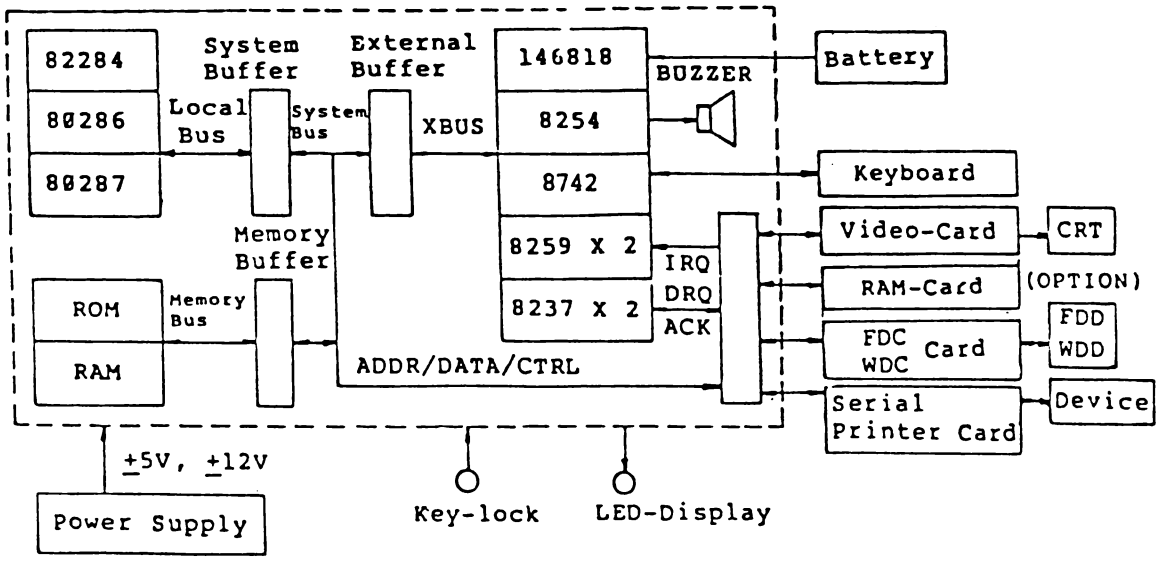
Pin No.	Description
0	Reset
1	Low/High speed status
2	not connected
3	GND
4	Keylock (keyboard inhibit)
5	GND

2.4 Variable capacity

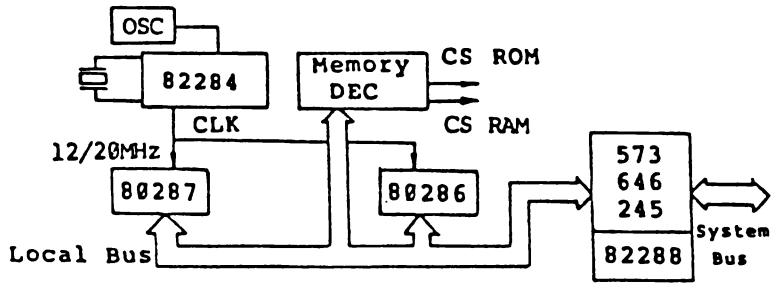
a) If there is no color, adjust the color burst signal at VC1.

b) Should the real-time clock keep inaccurate time, it can be corrected by adjusting the variable capacity at VC2.

2.5 Configuration

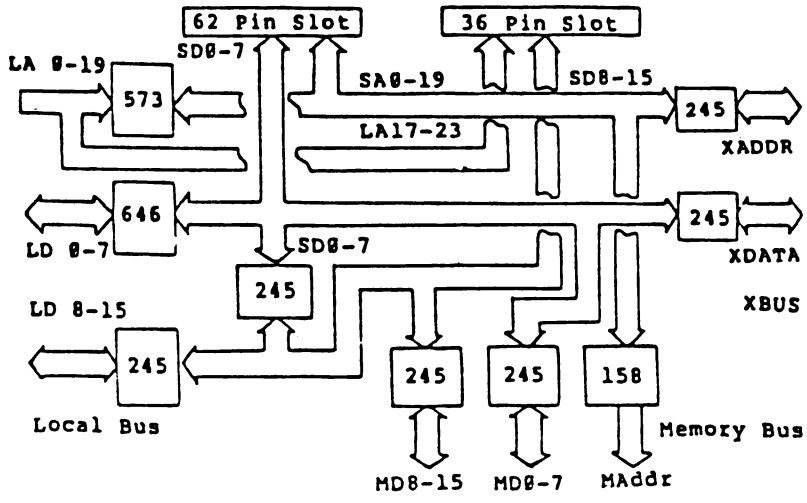


2.6 Functional description



Local-Bus:

82284:	Clock Generator
80286:	CPU/80287:NPX
82288:	Bus Controller



Svstem-Bus:

ADDR BUS:	SA0 - SA19
DATA BUS:	SD0 - SD15
CNTL BUS:	IOR/W, MR/W

DATA CONVERT

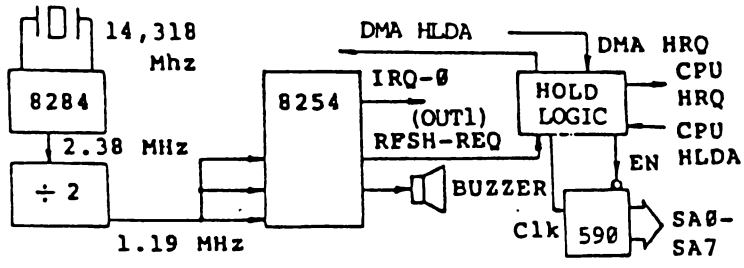
LD0 - 7	Access SD0 - SD7
LD8 - 15	Access SD0 - 7
LD0 - 15	Access SD0 - 7

(16-bit Bus <--> 8-bit Device)

2.7 Timer and Refresh

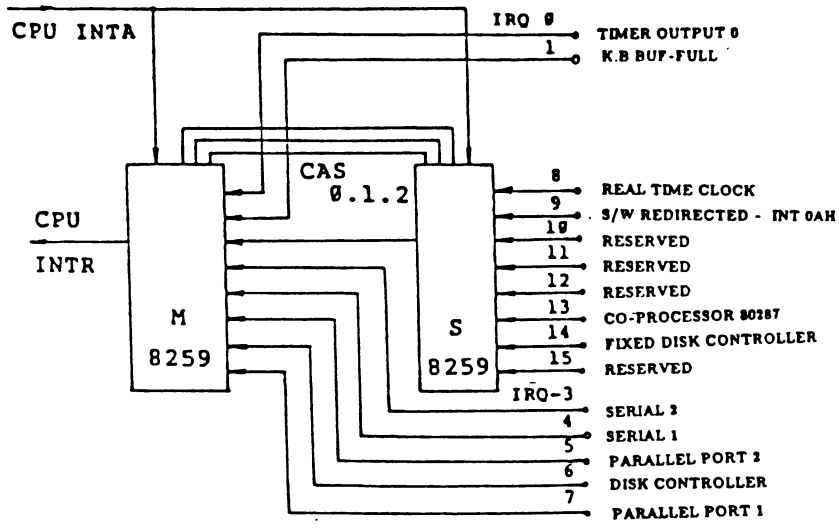
8254 :	System time base Sound system Refresh request
74590:	8-bit counter, support refresh address

CPU hold when refresh-req.

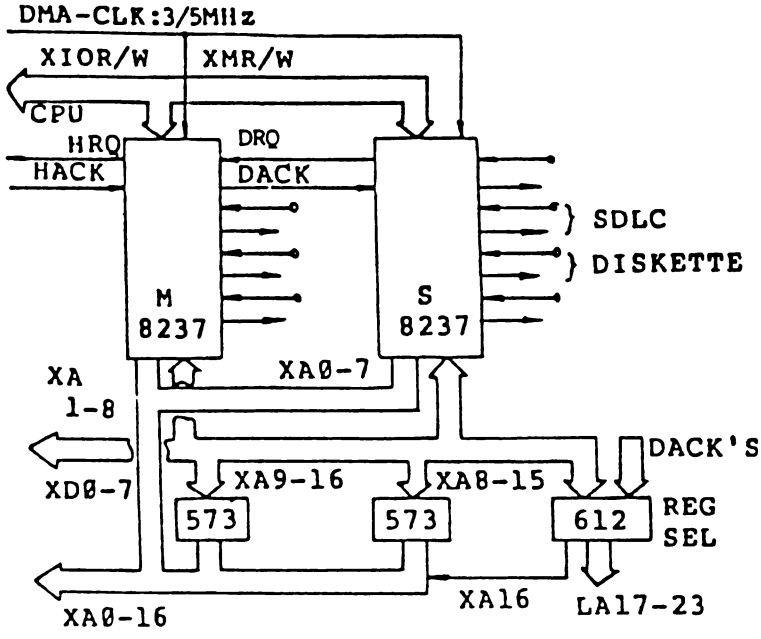


2.8 Interrupt

8259 PIC x 2
CASCADE MODE,
SUPPORT 15 LEVEL.



2.9 DMA



8237 DMA x 2 (CASCADE MODE)

Support 7 channels:

3 for 16-bit I/O <--> 16-bit bus mem

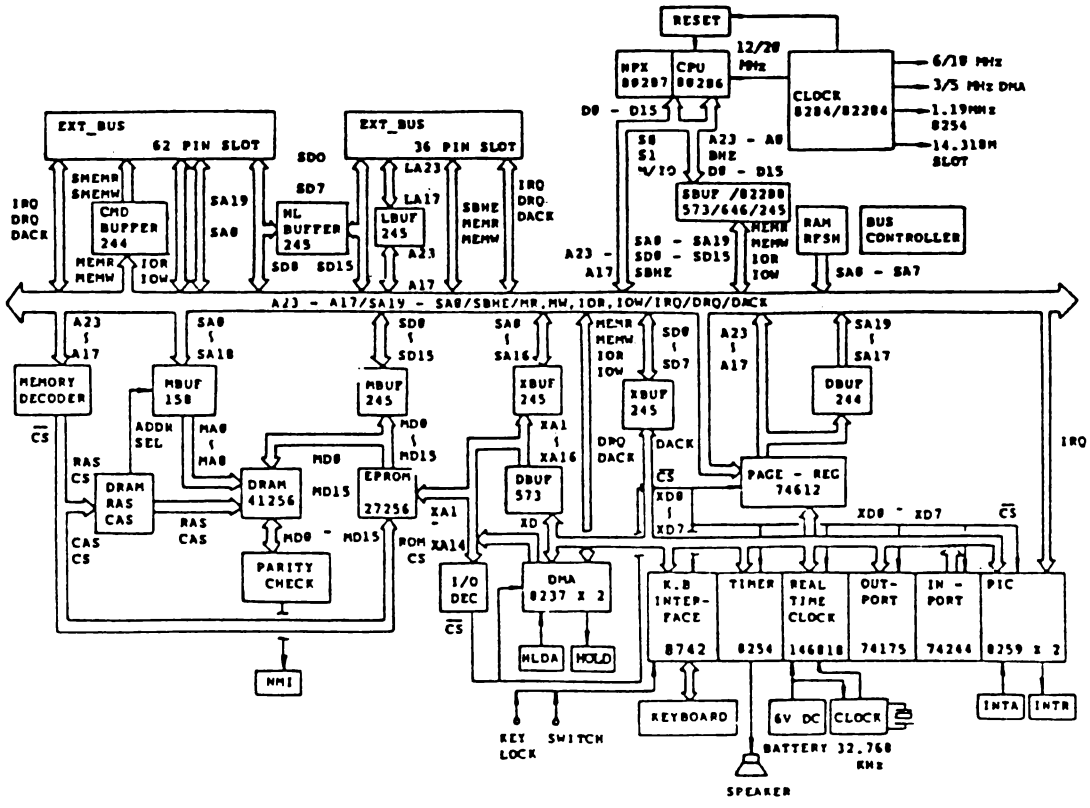
4 for 8-bit I/O <--> 8/16-bit bus mem

when DMA cycle,

LA17 - 23 come from 74LS612, (page-reg)

XA0 - 16 come from 8237

2.10 System Block



2.11 Specifications

1. CPU:
   80286, 10 MHz real and protected modes.

2. DMA:
   8237 x 2 (3 MHz), 7 DMA channels

3. IPC:
   8259 x 2 (15 interrupt levels)

4. Timer:
   8254 x 1 (3 channels)

5. ROM:
   27256 x 2 or 27128 x 4 (maximum 128 KB) four built-in 28 pin socket. In high speed mode ROM access time must not be less than 150 ns.

6. Backup:
   146818 x 1 (CMOS RAM and Clock/Calendar)

7. Co-processor:
   80287 x 1 numerical co-processor

8. Keyboard controller:
   8742 x 1 bi-directional serial interface

9. Slot:
   - 62-pin connector x 2 for 8-bit devices
   - 62-pin and 32-pin connectors x 6 for 8/16-bit devices

10. Operational Bus Cycle:
    - Normal cycle = 3 clock (1 TS + 2 TC) (1 wait)
    - 8-bit bus <--> 8-bit device = 6 CLK (4 wait states)
    - 16-bit bus <--> 16-bit device = 12 CLK (10 wait states)

11. Bus:
24 address lines (16 MB) and 16-bit data line.

12. RAM: 512 Kbytes DRAM (41256 x 18). IN high speed mode, access time must not be less than 120 ns.

2.12 I/O Address map

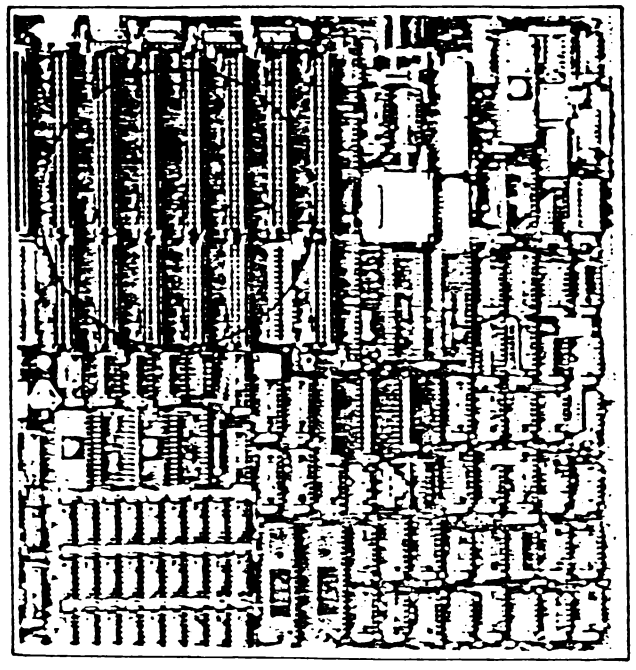
HEX range	Device
000 - 01f	DMA controller-1, 8237
020 - 03f	Interrupt controller-1, 8259
040 - 05f	Timer, 8254
060 - 06f	Keyboard controller, 8742
070 - 07f	Real-time clock, NMI mask
080 - 09f	DMA page register, 74LS612
0a0 - 0bf	Interrupt controller, 28259
0c0 - 0df	DMA controller-2, 8237
0f0 -	Clear 80287 busy
0f1 -	Reset 80287
0f8 - 0ff	

2.13 System memory map:

Address	Name	Function
000000	640 KB system	512 KB RAM (built-in) or 128 KB RAM card
09FFFF	Memory	
0A0000	128 KB video	reserved for graphics display
0BFFFF	RAM	Buffer
0C0000	128 KB I/O expansion	reserved for ROM on I/O adapters
0DFFFF	ROM	
0E0000	128 KB	0E0000 - 0EFFFF reserved on board
0FFFFF	System ROM	0F0000 - 0FFFFF 64 KB ROM
100000	Maximum memory	I/O channel memory expansion option
FDFFFF	15 MB	
FE0000	128 KB system	select to the same
FFFFFF	ROM	ROM as AE0000 - 0FFFFF

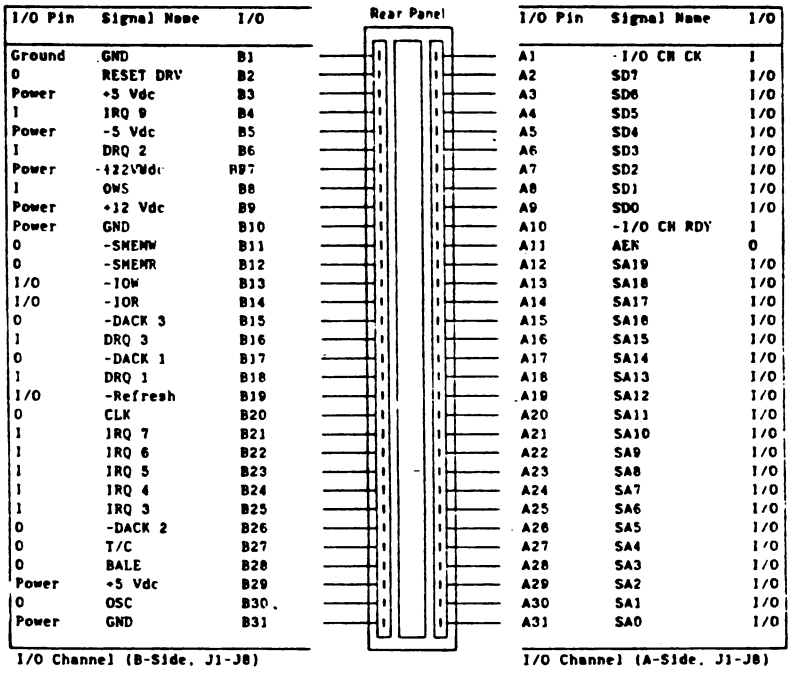
2.14 62- and 36-pin slot pin-out

Below is a figure showing the I/O channel connectors. These connectors have eight 62-pin and six 36-pin edge connector sockets.



Picture 8

Please note that the 36-pin connector is not present in two positions on the I/O channel. These positions only support 62-pin I/O bus adaptors.
Below is a figure showing the pin number and assignment for the I/O channel connectors slot 1 to slot 8.



I/O Pin	Signal Name	I/O
Ground	GND	B1
O	RESET DRV	B2
Power	+5 Vdc	B3
I	IRQ 9	B4
Power	-5 Vdc	B5
I	DRQ 2	B6
Power	-12Vdc	B7
I	OWS	B8
Power	+12 Vdc	B9
Power	GND	B10
O	-SMEMW	B11
O	-SMEMR	B12
I/O	-IOW	B13
I/O	-IOR	B14
O	-DACK 3	B15
I	DRQ 3	B16
O	-DACK 1	B17
I	DRQ 1	B18
I/O	-Refresh	B19
O	CLK	B20
I	IRQ 7	B21
I	IRQ 6	B22
I	IRQ 5	B23
I	IRQ 4	B24
I	IRQ 3	B25
O	-DACK 2	B26
O	T/C	B27
O	BALE	B28
Power	+5 Vdc	B29
O	OSC	B30
Power	GND	B31

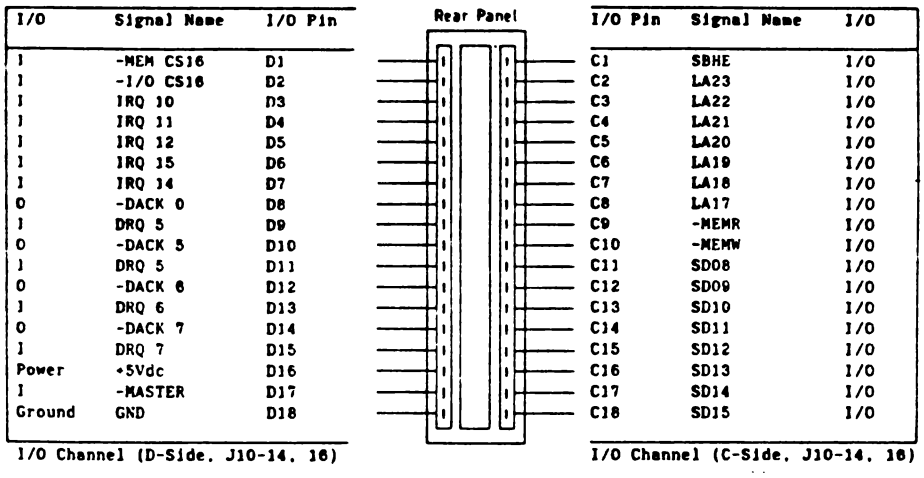
I/O Channel (B-Side, J1-J8)

Rear Panel

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (A-Side, J1-J8)

Below is a figure showing the pin numbering for the I/O channel connectors slot 10 to slot 14 and slot 16.



I/O	Signal Name	I/O Pin
I	-MEM CS16	D1
I	-I/O CS16	D2
I	IRQ 10	D3
I	IRQ 11	D4
I	IRQ 12	D5
I	IRQ 15	D6
I	IRQ 14	D7
O	-DACK 0	D8
I	DRQ 5	D9
O	-DACK 5	D10
I	DRQ 5	D11
O	-DACK 6	D12
I	DRQ 6	D13
O	-DACK 7	D14
I	DRQ 7	D15
Power	+5Vdc	D16
I	-MASTER	D17
Ground	GND	D18

I/O Channel (D-Side, J10-14, 16)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (C-Side, J10-14, 16)

Picture 10

2.15 I/O channel signal description

Below are the descriptions of the system board's I/O channel signals. The signal lines are TTL-compatible. The I/O adapters are designed with a maximum of 2 low-power Shottky (LS) loads per line.

SA0 - SA19 (I/O)

These address bits address memory and I/O devices within the system. The lines, in addition to LA17 - LA23, provide up to 16 MB of memory access. SA0 - 19 are gated on the system bus when 'bale' is high and are latched on the falling edge of 'bale'.
The signals are generated by the microprocessor or DMA controller, as well as by other such devices on the I/O channel.

LA17 - LA23 (I/O)

These signals address memory and I/O devices within the system, provide up to 16 MB of addressability and are valid when 'bale' is high. They are not latched during microprocessor cycles, so do not stay valid for the whole cycle. They are to generate memory decodes for 1 wait-state memory cycles. The decodes should be latched by I/O adapters on the falling edge of 'bale'.

Reset drive (0)

This is used to reset or initialize system logic during power-up time and during a low-line voltage outage. It is active high.

Clock

An 8-MHz system clock, it is a synchronous microprocessor cycle clock with a cycle time of 167 ns and has a 50% duty cycle. It should only be used for synchronization and is not intended for fixed frequeny.

Bale (0) (buffered)

This is provided by the 82288 bus controller and is used to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address when used with 'AEN'. 'Bale' is forced high during DMA cycles.

SD0 - SD15 (I/O)

These give bus bits 0 - 15 for microprocessor, memory and I/O devices. All 8-bit devices should use D0 - D7 for communications to the microprocessor, while 16-bit devices use D0 - D15.

I/O check (I)

This gives the system board parity information about memory and devices on the I/O channel. It indicates an uncorrectable system error when active.

I/O channel ready (I)

This pulled low by a memory or I/O device to lengthen their cycles. Any slow device on this line should drive it low as soon as it detects a valid address and a R/W command. Do not hold this signal low for more than 2,5 microseconds.

IRQ-7, IRQ-12 and IRQ-15

These interrupt requests signal the microprocessor that an I/O device needs attention. IRQ9 - 12 and IRQ14 - 15 have highest priority (9 is highest) and 3 - 7 have lowest priority (7 is lowest). Interrupt requests are generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request.

I/O Read and Write

These signals tell an I/O device to drive their data onto data bus. They may be driven by any microprocessor or DMA controller in the system. Both signals are active low.

SMEMR(O), MEMR((I/O) and
SMEMW(O), MEMW(I/O)

The first two signals tell the memory devices to drive the data onto data bus, while the last two tell the memory devices to store the data present on the data bus. SMEMR and SMEMW are active only when the memory decode is within the low 1 MB of the memory space. MEMR and MEMW may be driven by any microprocessor or DMA controller in the system. SMEMR and SMEMW are derived from MEMR and MEMW, respectively, and the decode of the low 1 MB of memory. All of these signals are active low.

DRQ0 - 3 and DRQ5 - 7 (I)

These DMA requests are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service or control of system. DRQ0 has highest priority and DRQ7 has the lowest. A request is generated by bringing a DRQ line to an active level. The lines must be held high until the corresponding DMA request acknowledge goes active. DRQ5 - 7 perform 16-bit transfers.

Dack0 - 3 and Dack5 - 7 (O)

These DMA acknowledge requests are active low and are used to acknowledge DMA requests 0 - 7.

AEN

Address enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When AEN is active the DMA controller has control of the address bus and the data-bus Read and Write command lines (memory and I/O).

Refresh (I/O)

This signal is used to show a refresh cycle and can be driven by a microprocessor on the I/O channel.

Terminal/Count (O)

Terminal count gives a pulse when terminal count for any DMA channel is realized.

Sbhe (I/O)

The Bus High Enable system shows a transfer of data on the upper byte of the data bus, SD8 - 15. Sixteen-bit devices use this system to condition data bus buffers tied to SD8 - 15.

Master (I)

This is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and get a DACK. An I/O microprocessor might pull this signal low when it receives the DACK so it can control the system address, data and control lines. When MASTER is low, the I/O microprocessor must wait one clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. System memory may be lost if this signal is held low for more than 15 microseconds.

Mem CS16 and I/O CS16 (I)

Memory 16 Chip Select and I/O 16-bit Chip Select tell the system board if the present data transfer is a 1 wait-state, 16-bit, memory or I/O cycle. Mem CS16 must be derived from the decode of LA17 - 23, while I/O CS16 is derived from an address code. I/O CS16 is active low. Both of these selects should be driven with an open collector or tristate driver capable of sinking 20 mA.

Osc (O)

The Oscillator is a high speed clock with a period of 70 nanoseconds (14,3181 MHz). It is not synchronous with the system clock. It has a 50% duty cycle.

2.16 Jumper setting for speed and RAM configuration

a)Jumper setting for speed

Speed: The operating speed of the system is switchable between 6 MHz and 10 MHz.

The clock processing speed can be changed by one of the following methods.

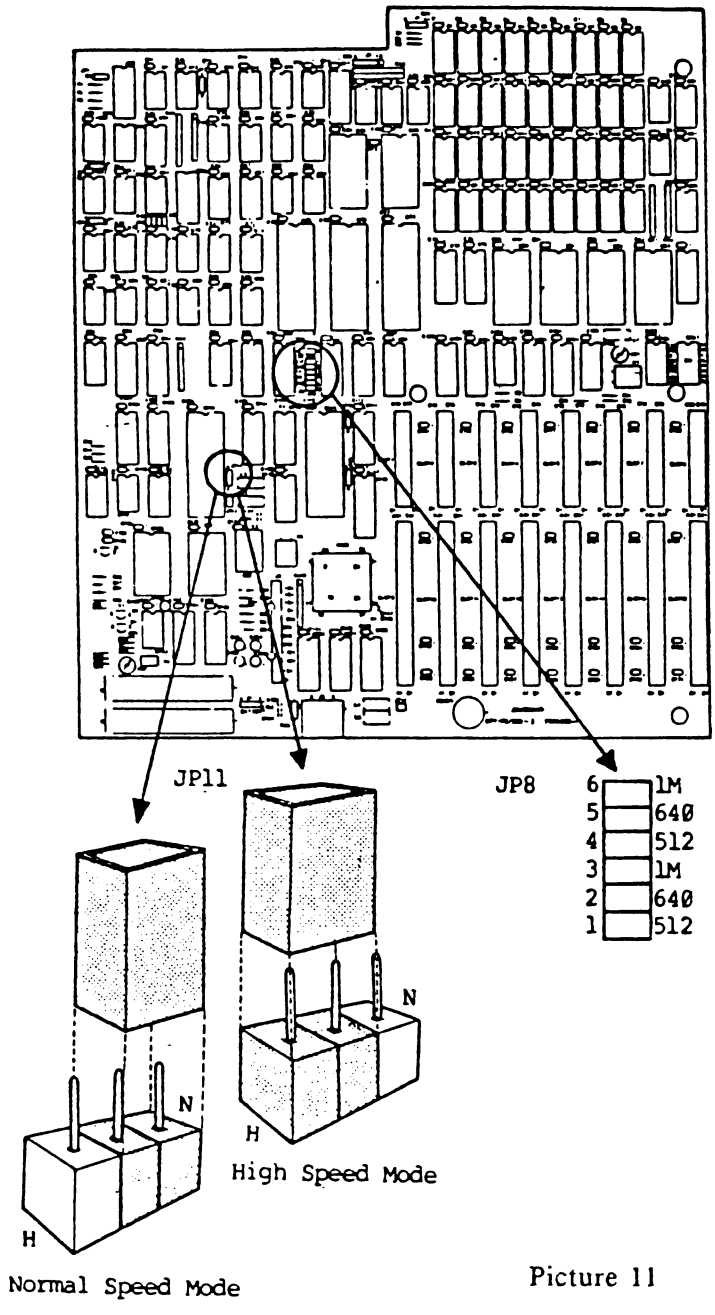
1. The operating speed can be switched by inserting a short plug to the 3-pin jumper JP11 on the system board. The location of JP11 is shown in the picture 11 below.

When the shorting plug is inserted nearer to the position marked N, the normal speed mode is selected. Inserting the plug nearer to the position marked H, selects the high speed mode. See picture 11 below.

2. Pressing the three keys, CTRL - ALT - +, together switches the system from the current to the other speed mode. This method may only work, if no keyboard driver is installed.

The jumper JP1 is used to generate a 1 wait state in memory cycle in case the system is switched to normal speed. When using high speed the jumper position doesn't matter.

JP1 in position A: no wait state in memory cycle
JP1 in position B: one wait state in memory cycle


JP11
JP8
6 1M
5 640
4 512
3 1M
2 640
1 512
N
H
High Speed Mode
N
H
Normal Speed Mode

Picture 11

b) Jumper setting for RAM configuration

Memory: 1 MB on-board DRAM

In the picture 11 above, the jumper module JP8 is used to set the system to match the amount of RAM installed on the system board. For example, when the system is installed with a total of 512 KB of RAM, the shorting plugs are inserted to locations 1 and 4 of JP8.

Note: If you expand the RAM to 1 MB, the DOS can only manage the range of 512/640 KB on board. The additional 512 KB RAM is addressed by special 80286 commands.
A few programs use this range for data memory or as a RAM drive (see DOS 3.2 manual).

The jumper JP7 is used to change the base memory size from 512 KB to 256 KB in case that jumper JP8 is in position marked with 512. The following table shows the RAM size:

position JP7	position JP8	base size	external size
B	512	256 KB	0 KB
A	512	512 KB	0 KB
A	640	640 KB	0 KB
A	1M	512 KB	512 KB

Note: If you change the system configuration you have to run the set-up program to correct the system's information.

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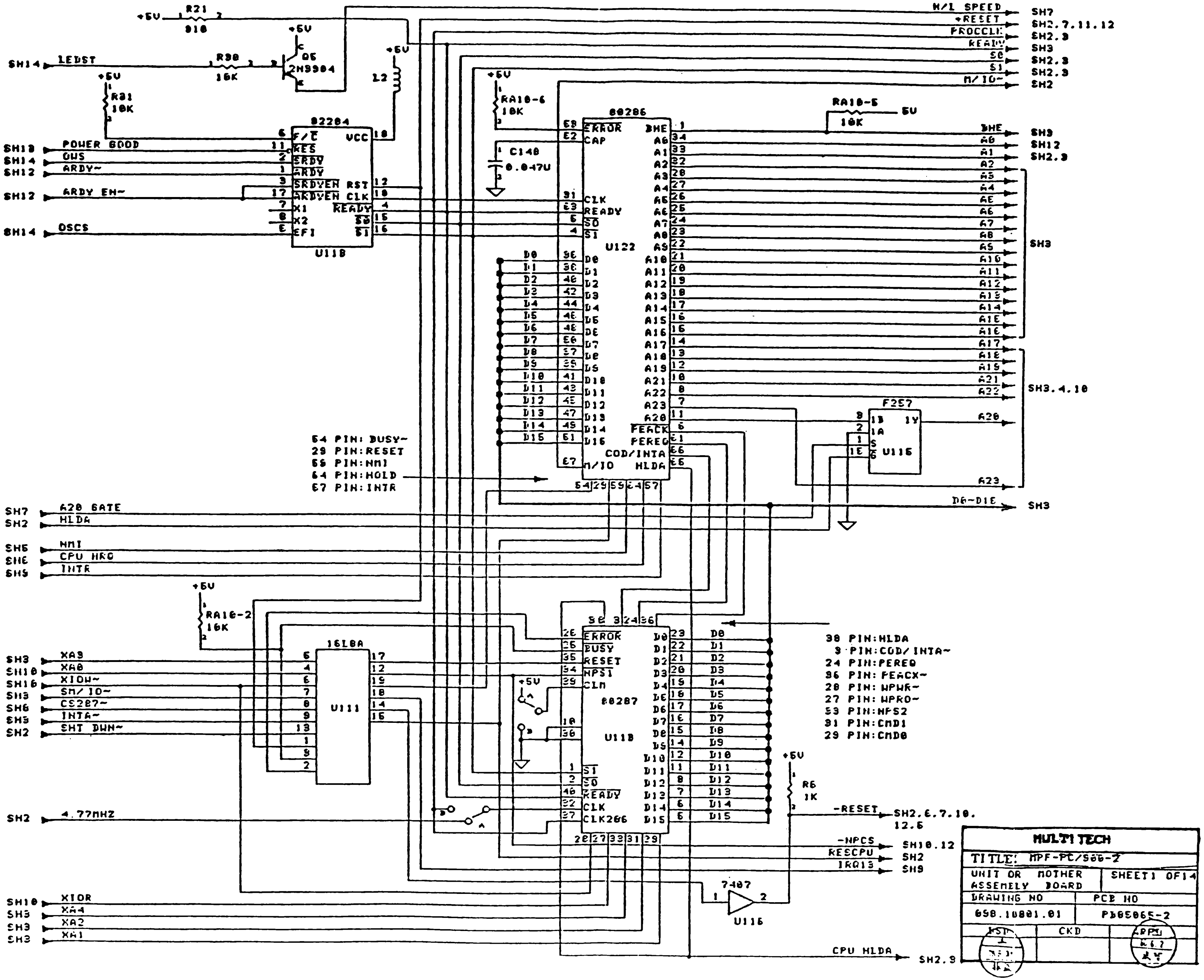
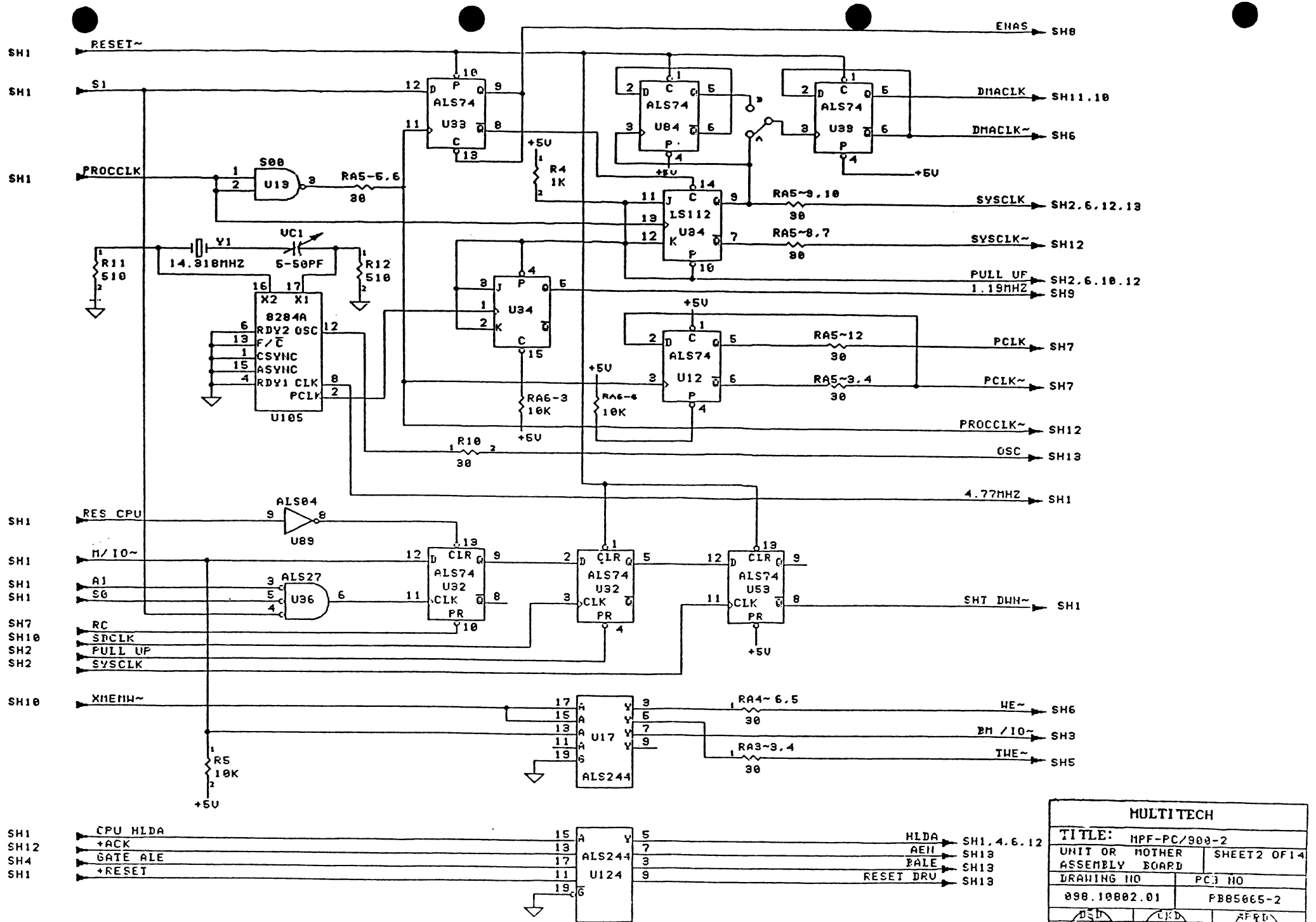
MS-DOS is a trademark of Microsoft Corporation.

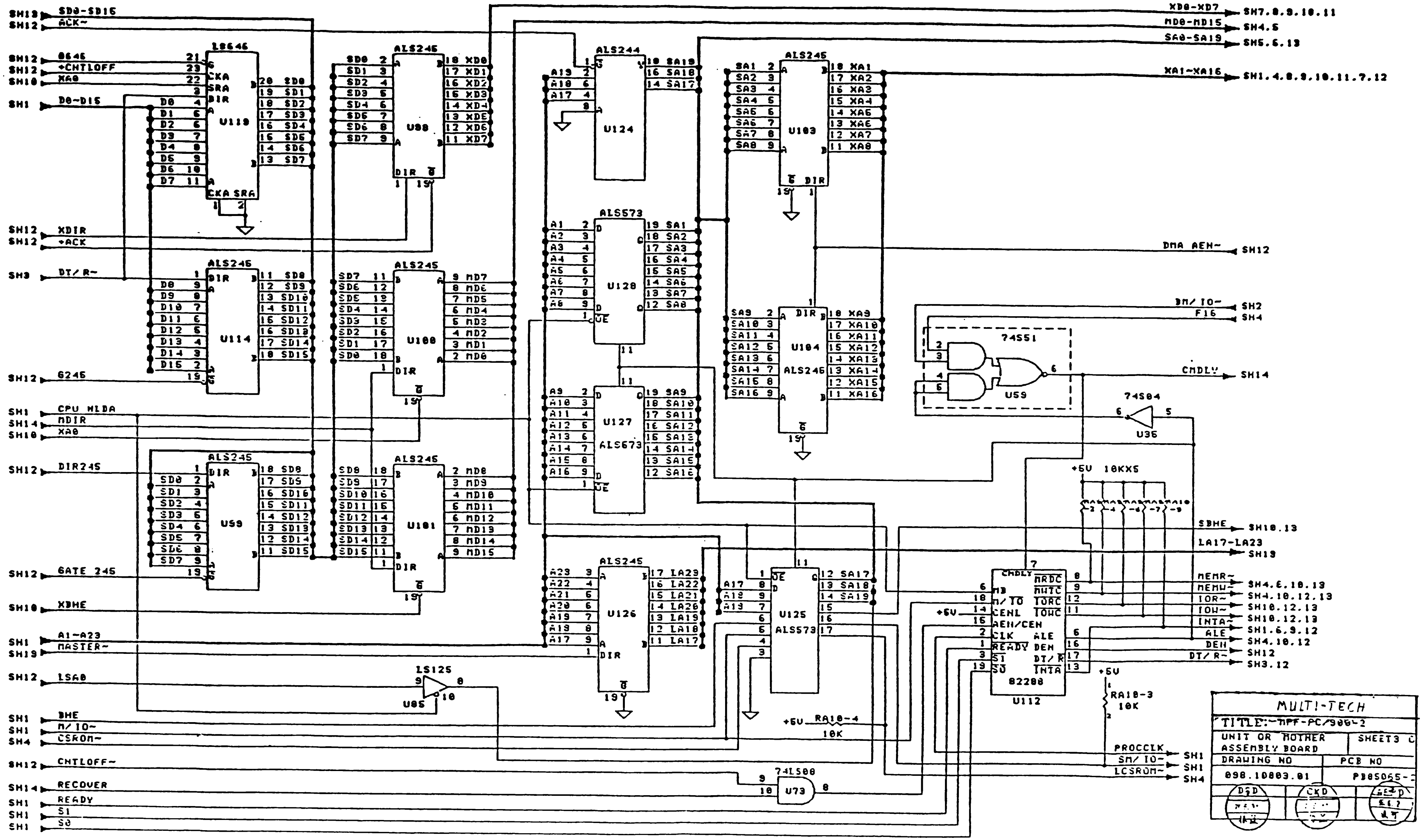
UNIX is a trademark of Bell Laboratories.



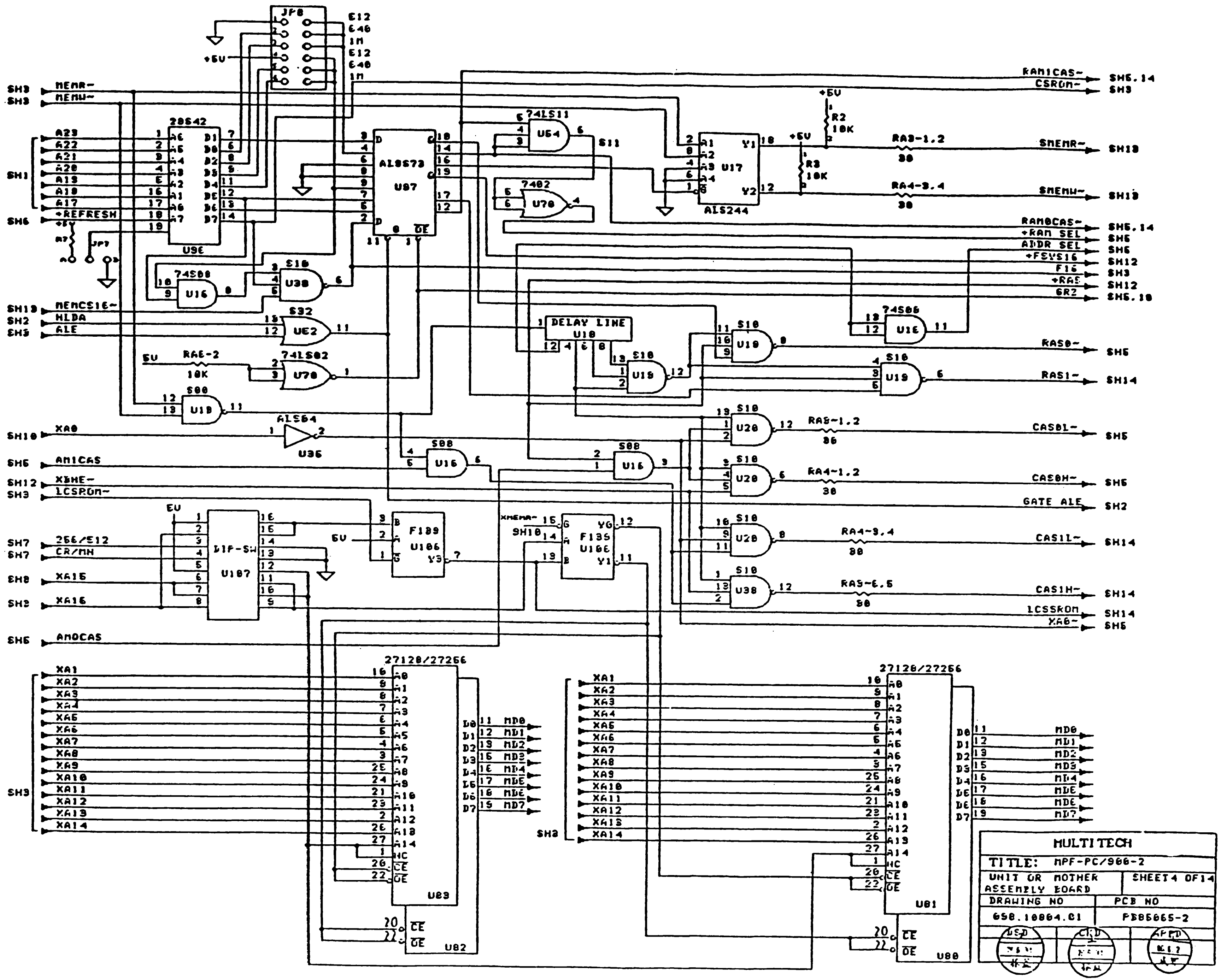
M/I SPEED
+RESET
PROCCLK
READY
S0
S1
M/IO~
SH7
SH2.7.11.12
SH2.9
SH3
SH2.9
SH2.9
SH2
LEDST
R21
910
R30
10K
Q5
2N3904
R31
10K
L2
+5V
82284
U118
POWER GOOD
OWS
ARDY~
ARDY EN~
OSCS
RA10-6
10K
C140
0.047U
80286
U122
RA10-5
10K
BHE
A0
A1
A2
F257
U115
A20
A23
D0-D15
SH3
SH3.4.10
54 PIN: BUSY~
29 PIN: RESET
55 PIN: NMI
64 PIN: HOLD
57 PIN: INTR
A20 GATE
HLDA
NMI
CPU HRQ
INTR
RA10-2
10K
16L8A
U111
XA3
XA0
XIOW~
SM/IO~
CS287~
INTA~
SHT DWN~
80287
U118
30 PIN: HLDA
3 PIN: COD/INTA~
24 PIN: PEREQ
36 PIN: PEACK~
28 PIN: NPWR~
27 PIN: NPRD~
53 PIN: NPS2
31 PIN: CMD1
29 PIN: CMD0
4.77MHZ
R6
1K
-RESET
SH2.6.7.10.12.6
-NPCS
RESCPU
IRQ13
SH10.12
SH2
SH9
7407
U115
CPU HLDA
SH2.9
XIOR
XA4
XA2
XA1
MULTITECH
TITLE: MPF-PC/500-2
UNIT OR ASSEMBLY: MOTHER BOARD
SHEET1 OF14
DRAWING NO: 658.10801.01
PCB NO: P305065-2
DSN
CKD
APPD



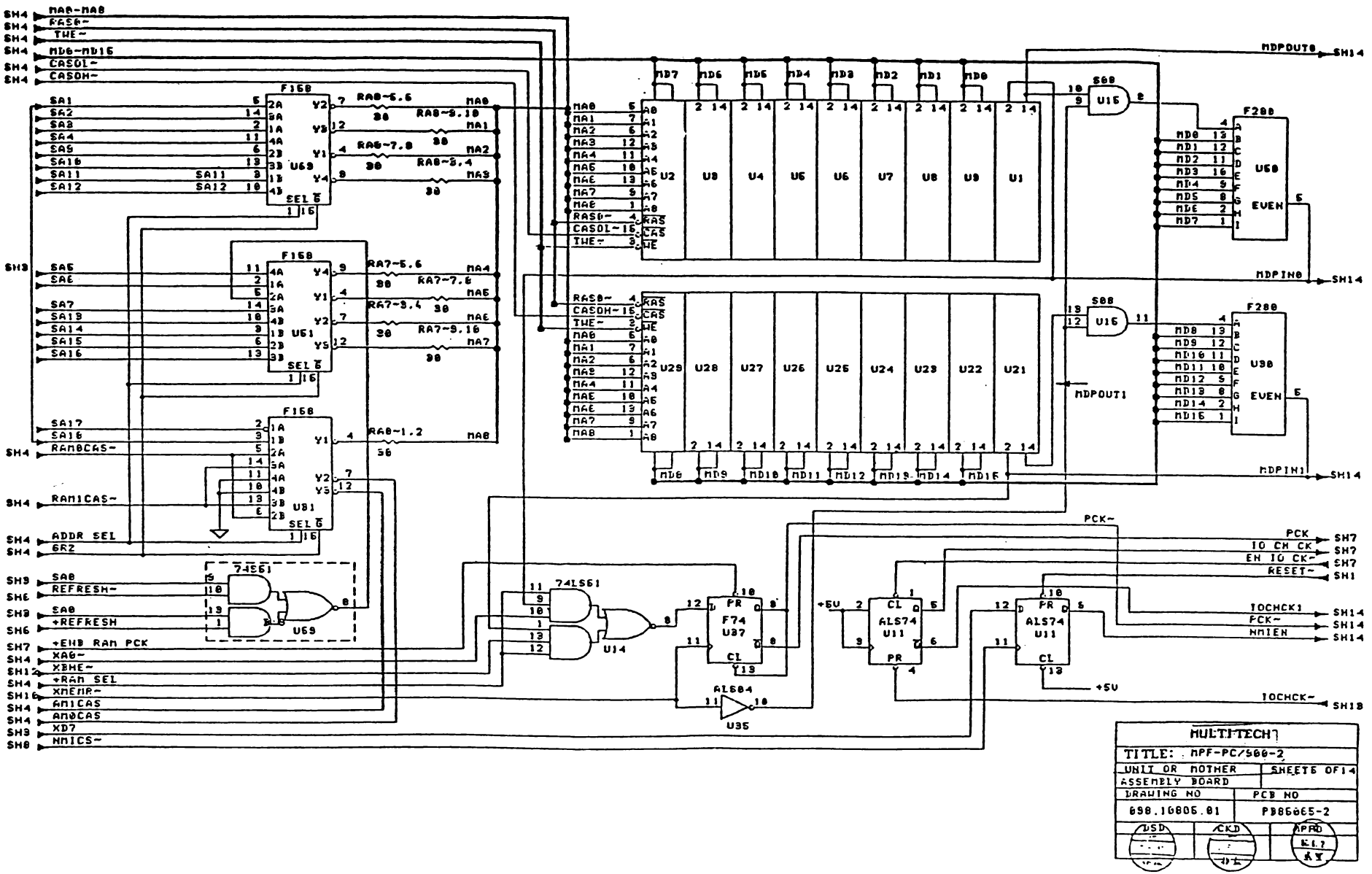
MULTITECH	
TITLE: MPF-PC/900-2	
UNIT OR MOTHER ASSEMBLY BOARD	SHEET2 OF14
DRAWING NO	PCB NO
898.10802.01	PB85065-2
DSN	CHK APRD



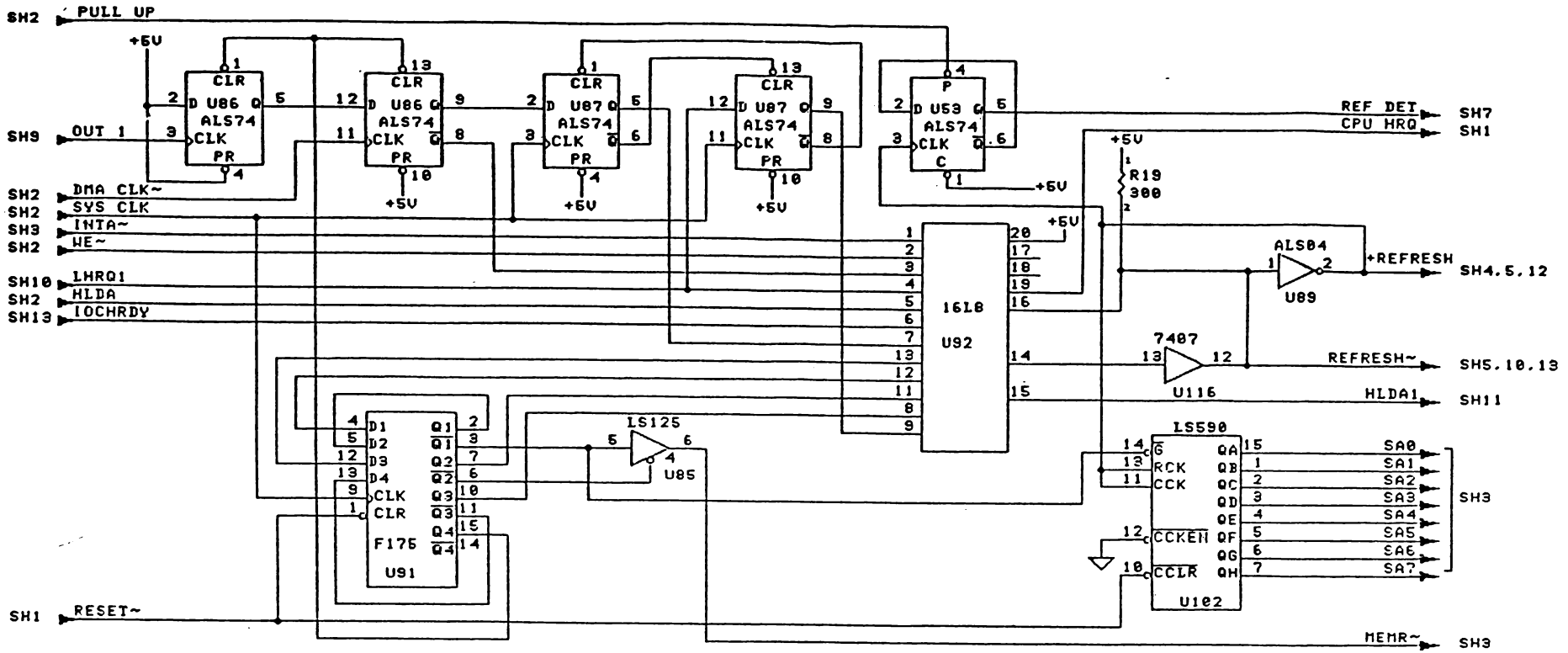
SD0-SD15
ACK~
8646
+CNTLOFF
XA0
D0-DIS
XDIR
+ACK
DT/R~
G245
CPU HLDA
MDIR
DIR245
GATE 245
XBHE
A1-A23
MASTER~
LSA0
BHE
M/IO~
CSROM~
CNTLOFF~
RECOVER
READY
S1
S0
18646
U119
ALS245
U114
U59
U98
U100
U101
ALS244
U124
ALS573
U128
U127
ALS673
U126
U125
U103
U104
ALS246
74S51
U59
74S04
U35
LS125
U85
74LS00
U73
82288
U112
+5V
10KX5
RA10-3
10K
RA10-4
XD0-XD7
SH7.8.9.10.11
MD0-MD15
SH4.5
SA0-SA19
SH5.6.13
XA1-XA16
SH1.4.8.9.10.11.7.12
DMA AEN~
SH12
DM/IO~
SH2
F16
SH4
CMDLY
SH14
SBHE
SH10.13
LA17-LA23
SH19
MEMR~
SH4.6.10.13
MEMW~
SH4.10.12.13
IOR~
SH10.12.13
IOW~
SH10.12.13
INTA~
SH1.6.9.12
ALE
SH4.10.12
DEN
SH12
DT/R~
SH3.12
PROCCLK
SH1
SM/IO~
SH1
LCSROM~
SH4
MULTI-TECH
TITLE: MPF-PC/900-2
UNIT OR MOTHER ASSEMBLY BOARD
SHEET3
DRAWING NO
PCB NO
098.10803.01
P385065-
DSD
CKD



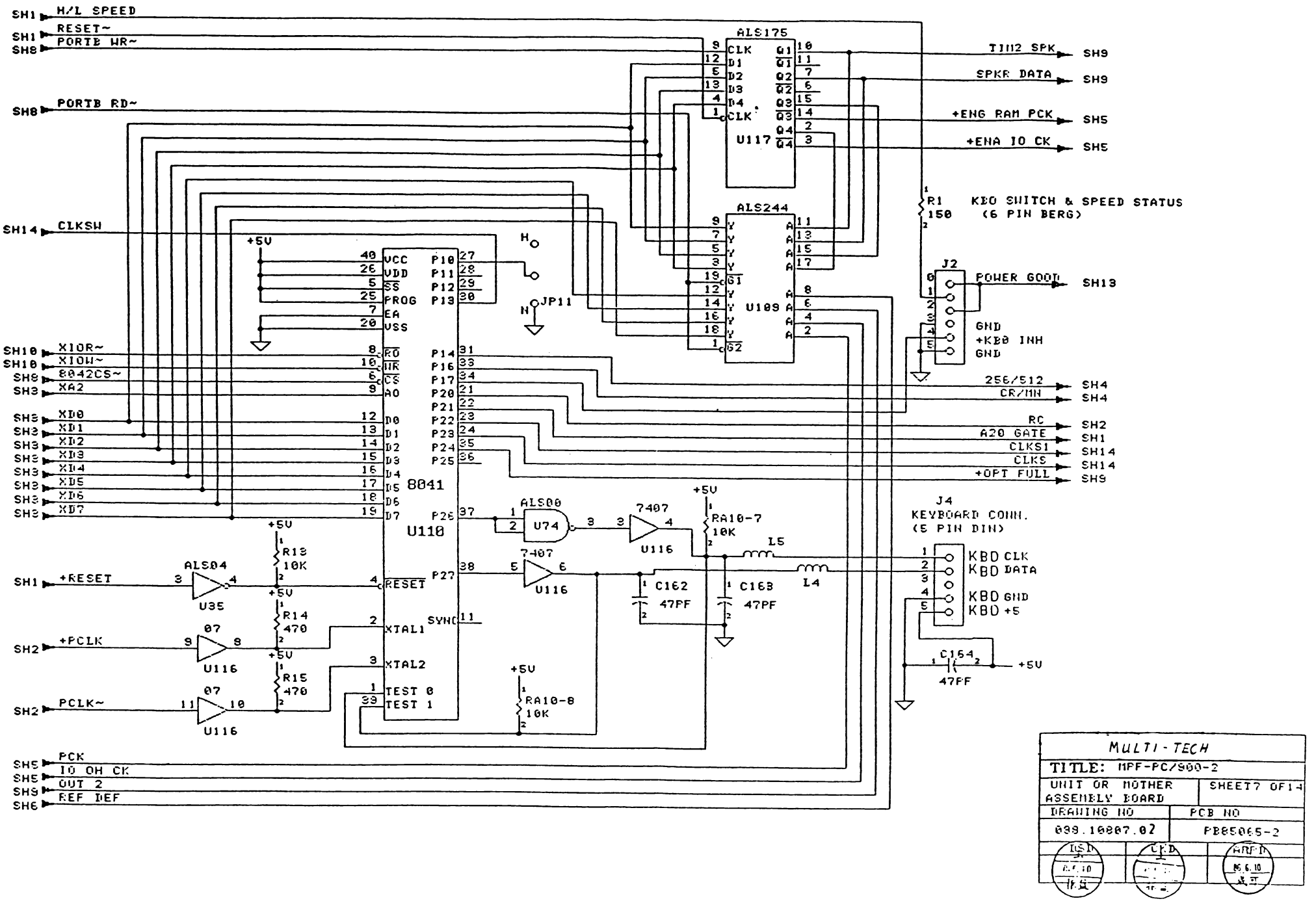
MEMR-
MEMW-
A23
A22
A21
A20
A19
A18
A17
+REFRESH
28S42
U96
JP8
E12
E40
1M
74LS11
U54
7402
U70
ALS573
U97
ALS244
U17
R2 10K
R3 10K
+5V
RA3-1.2 30
RA4-3.4 30
SMEMR-
SMEMW-
RAMICAS-
CSROM-
RAMOCAS-
+RAM SEL
ADDR SEL
+FSYS16
F16
+RAS
GR2
MEMCS16-
HLDA
ALE
74S08
U16
S10
U38
S32
UE2
74LS02
U70
RAE-2 10K
S00
U19
XA0
ALS04
U36
AMICAS
XBHE-
1CSROM-
DELAY LINE
U18
74S86
U16
RAS0-
RAS1-
CAS0L-
CAS0H-
GATE ALE
CAS1L-
CAS1H-
1CSSROM
XA6-
RAS-1.2 30
RA4-1.2 30
RA4-3.4 30
RAS-5.6 30
256/512
CR/MN
XA15
XA16
DIP-SW
U107
F139
U106
F138
U108
AMOCAS
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
XA13
XA14
27128/27256
U83
U82
U81
U80
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
SH1
SH2
SH3
SH5
SH6
SH7
SH8
SH10
SH12
SH14
MULTITECH
TITLE: MPF-PC/900-2
UNIT OR MOTHER ASSEMBLY BOARD
SHEET4 OF14
DRAWING NO
PCB NO
650.10004.01
F805665-2

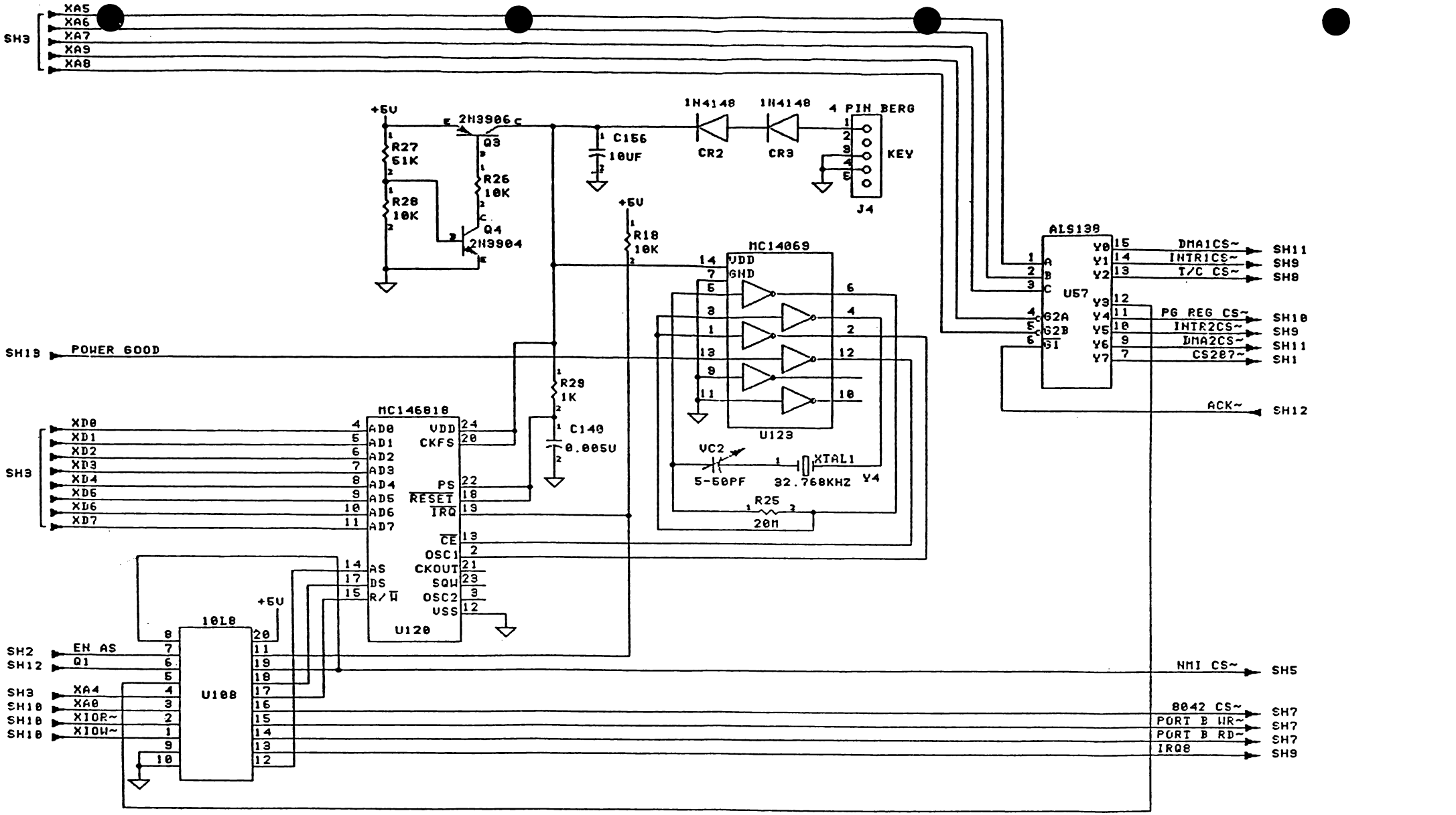


MULTITECH		
TITLE: MPF-PC/500-2		
UNIT OR MOTHER ASSEMBLY BOARD		SHEETS OF 14
DRAWING NO		PCB NO
698.10805.01		PB86865-2
DSD	CKD	APRD

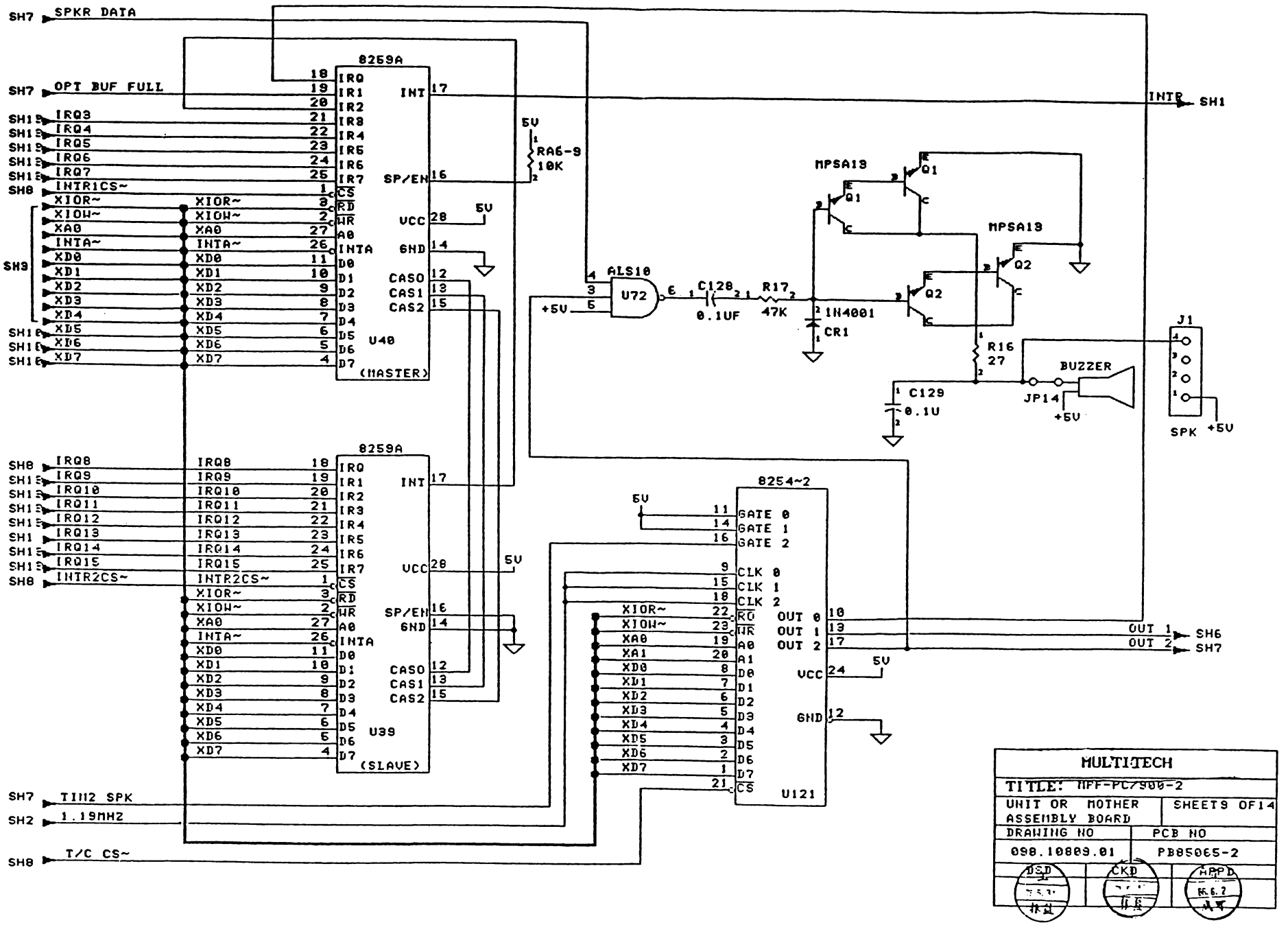


MULTITECH		
TITLE MPF-PC/900-2		
UNIT OR ASSEMBLY MOTHER BOARD		SHEET 6 OF 14
DRAWING NO 098.10806.01	PCB NO PB85065-2	
DSD	CKD	APPD

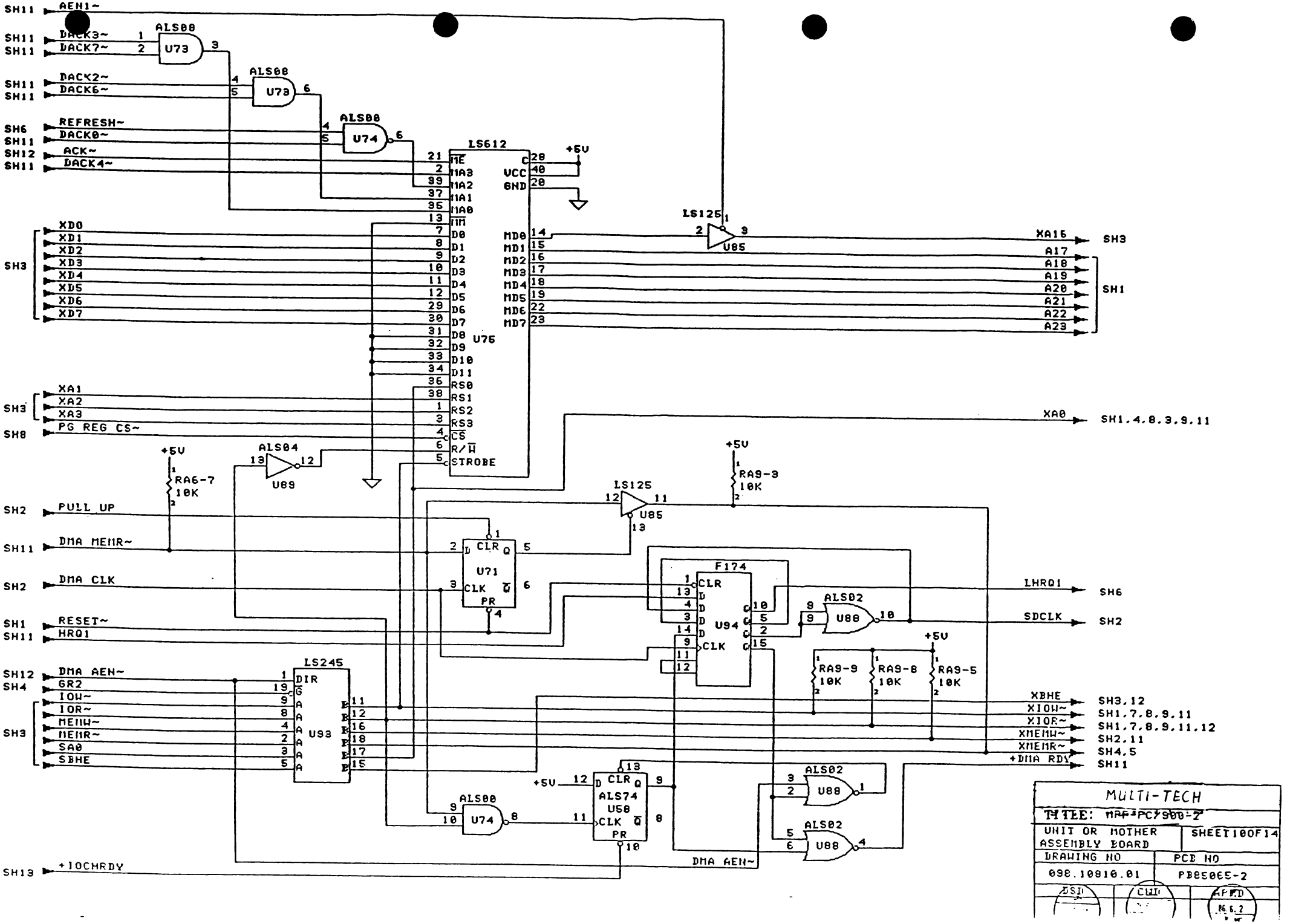

SH1 H/L SPEED
SH1 RESET~
SH8 PORTB WR~
SH8 PORTB RD~
SH14 CLKSW
SH10 XIOR~
SH10 XIOW~
SH8 8042CS~
SH3 XA2
SH3 XD0
SH3 XD1
SH3 XD2
SH3 XD3
SH3 XD4
SH3 XD5
SH3 XD6
SH3 XD7
SH1 +RESET
SH2 +PCLK
SH2 PCLK~
SH5 PCK
SH5 IO CH CK
SH5 OUT 2
SH6 REF DET
ALS175
U117
ALS244
U109
TIM2 SPK
SPKR DATA
+ENG RAM PCK
+ENA IO CK
R1 150
KBD SWITCH & SPEED STATUS
(6 PIN BERG)
J2
POWER GOOD
GND
+KBD INH
GND
256/512 CR/MN
RC
A20 GATE
CLKSI
CLKS
+OPT FULL
J4
KEYBOARD CONN.
(5 PIN DIN)
KBD CLK
KBD DATA
KBD GND
KBD +5
8041
U110
JP11
ALS00
U74
7407
U116
ALS04
U35
RA10-7 10K
RA10-8 10K
R13 10K
R14 470
R15 470
L5
L4
C162 47PF
C163 47PF
C164 47PF
+5V
MULTI-TECH
TITLE: MPF-PC/900-2
UNIT OR MOTHER ASSEMBLY BOARD
SHEET 7 OF 14
DRAWING NO 039.10007.02
PCB NO PB85065-2

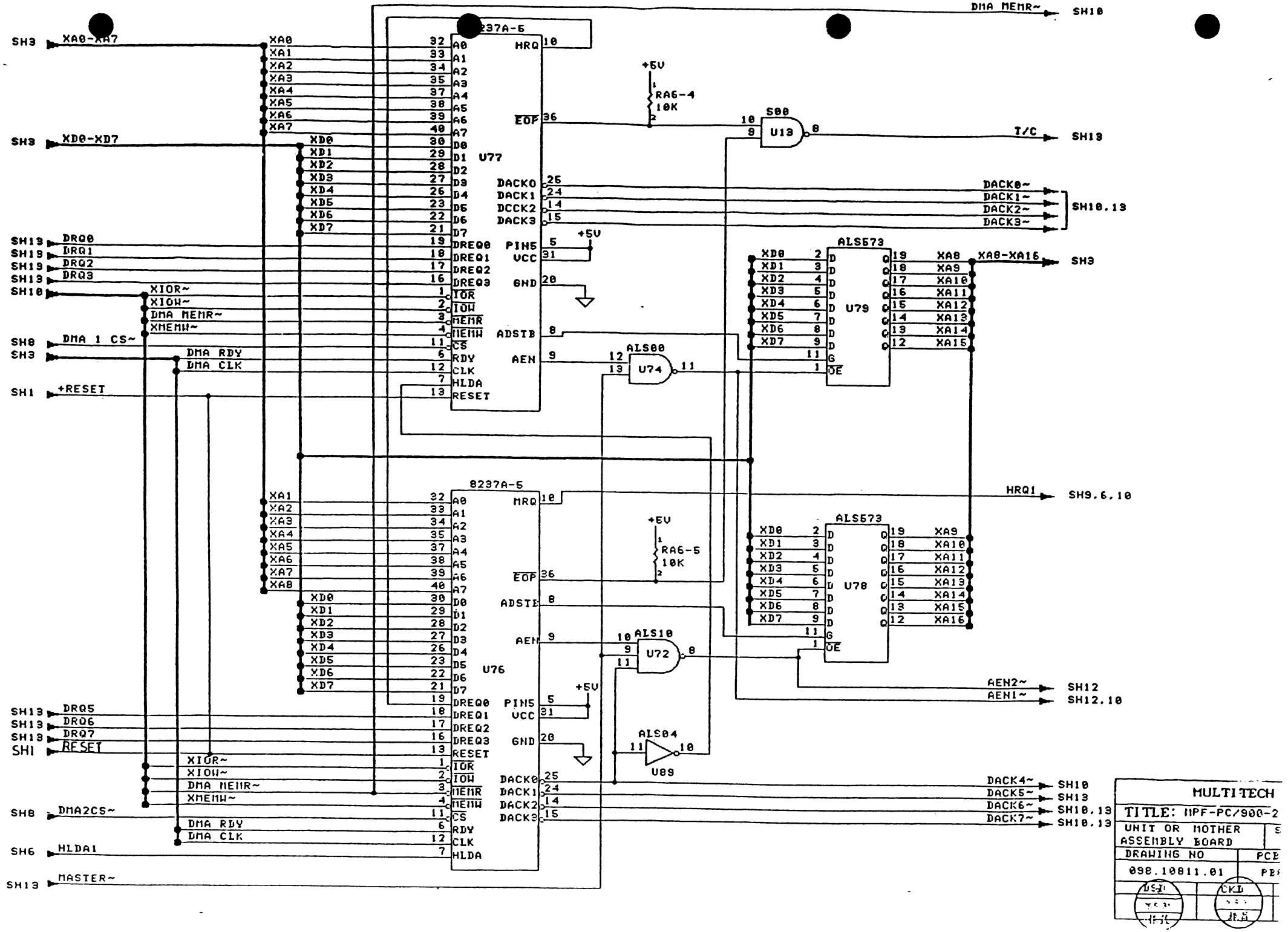


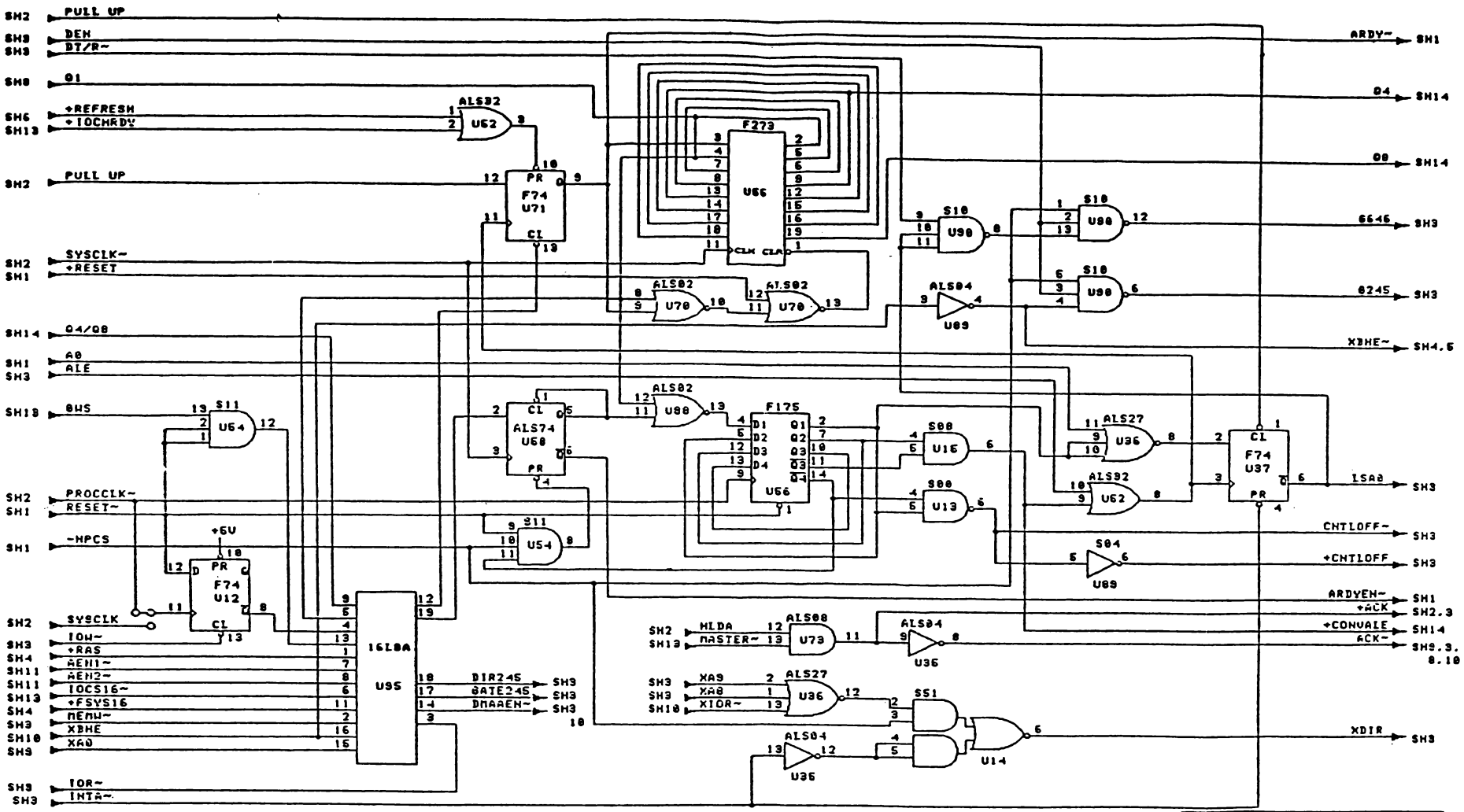
MULTITECH	
TITLE: MPF-PC/900-2	
UNIT OR MOTHER ASSEMBLY BOARD	SHEET 8 OF 14
DRAWING NO	PCB NO
098.10808.01	PB85065-2
DSN	CHD APPD



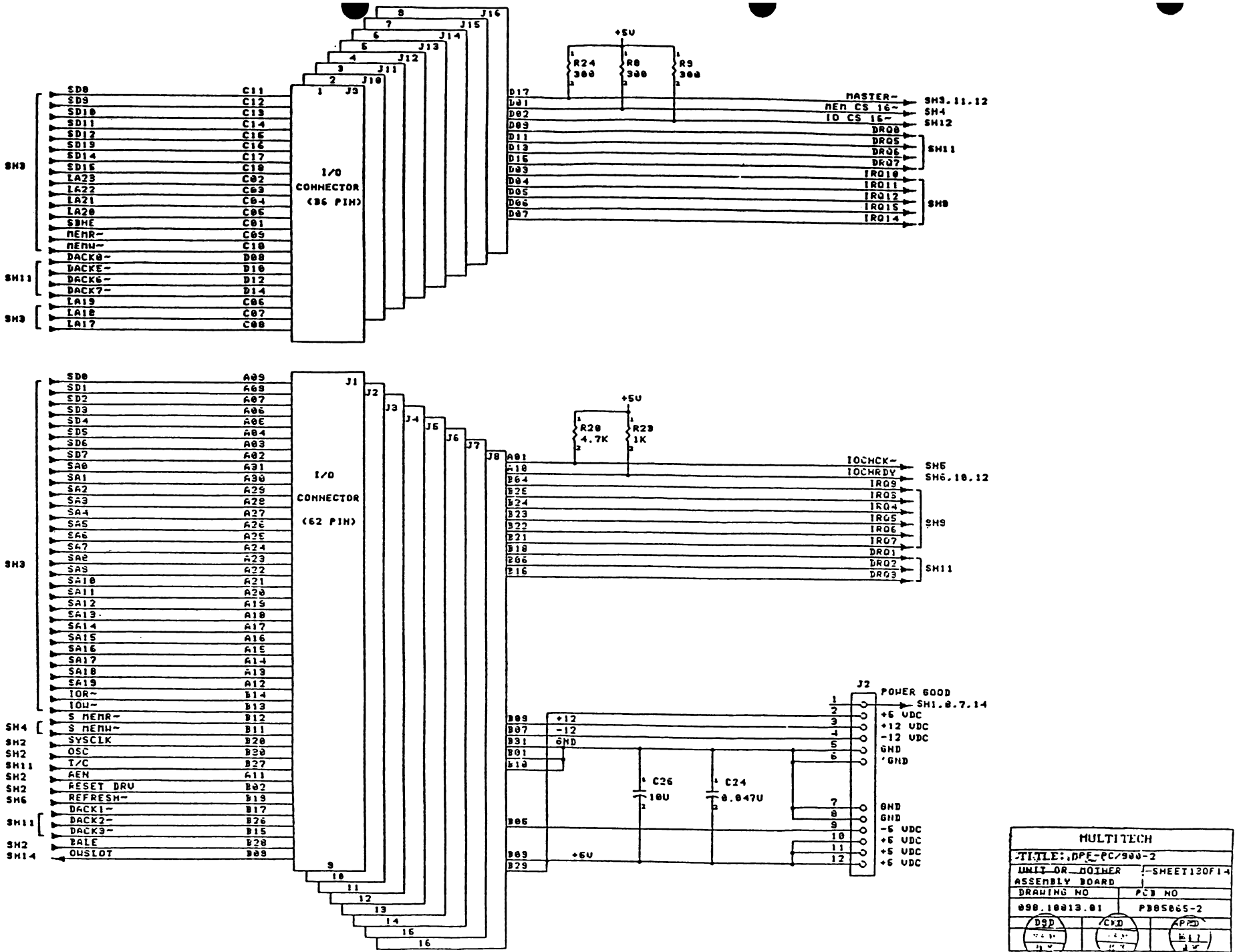
MULTITECH	
TITLE: MFF-PC/900-2	
UNIT OR MOTHER ASSEMBLY BOARD	SHEETS OF 14
DRAWING NO	PCB NO
098.10809.01	PB85065-2
DSD	CKD / APPD


SH11 AEN1~
SH11 DACK3~
SH11 DACK7~
ALS08 U73
SH11 DACK2~
SH11 DACK6~
ALS08 U73
SH6 REFRESH~
SH11 DACK0~
SH12 ACK~
SH11 DACK4~
ALS08 U74
LS612
+5V
VCC
GND
U76
SH3 XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
SH3 XA1 XA2 XA3
SH8 PG REG CS~
RS0 RS1 RS2 RS3 CS R/W STROBE
LS125 U85
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7
XA16 A17 A18 A19 A20 A21 A22 A23
SH3
SH1
XA0
SH1.4.8.3.9.11
+5V
RA6-7 10K
ALS04 U89
SH2 PULL UP
SH11 DMA MEMR~
SH2 DMA CLK
SH1 RESET~
SH11 HRQ1
U71
F174 U94
ALS02 U88
LHRQ1
SH6
SDCLK
SH2
RA9-3 10K
RA9-9 10K
RA9-8 10K
RA9-5 10K
SH12 DMA AEN~
SH4 GR2
SH3 IOW~ IOR~ MEMW~ MEMR~ SA0 SBHE
LS245 U93
XBHE SH3.12
XIOW~ SH1.7.8.9.11
XIOR~ SH1.7.8.9.11.12
XMEMW~ SH2.11
XMEMR~ SH4.5
+DMA RDY SH11
ALS74 U58
ALS08 U74
SH13 +IOCHRDY
DMA AEN~
MULTI-TECH
TITLE: MAP-PC/900-2
UNIT OR MOTHER ASSEMBLY BOARD
SHEET 10 OF 14
DRAWING NO 090.10810.01
PCB NO PB85065-2
DSN CHK APPD

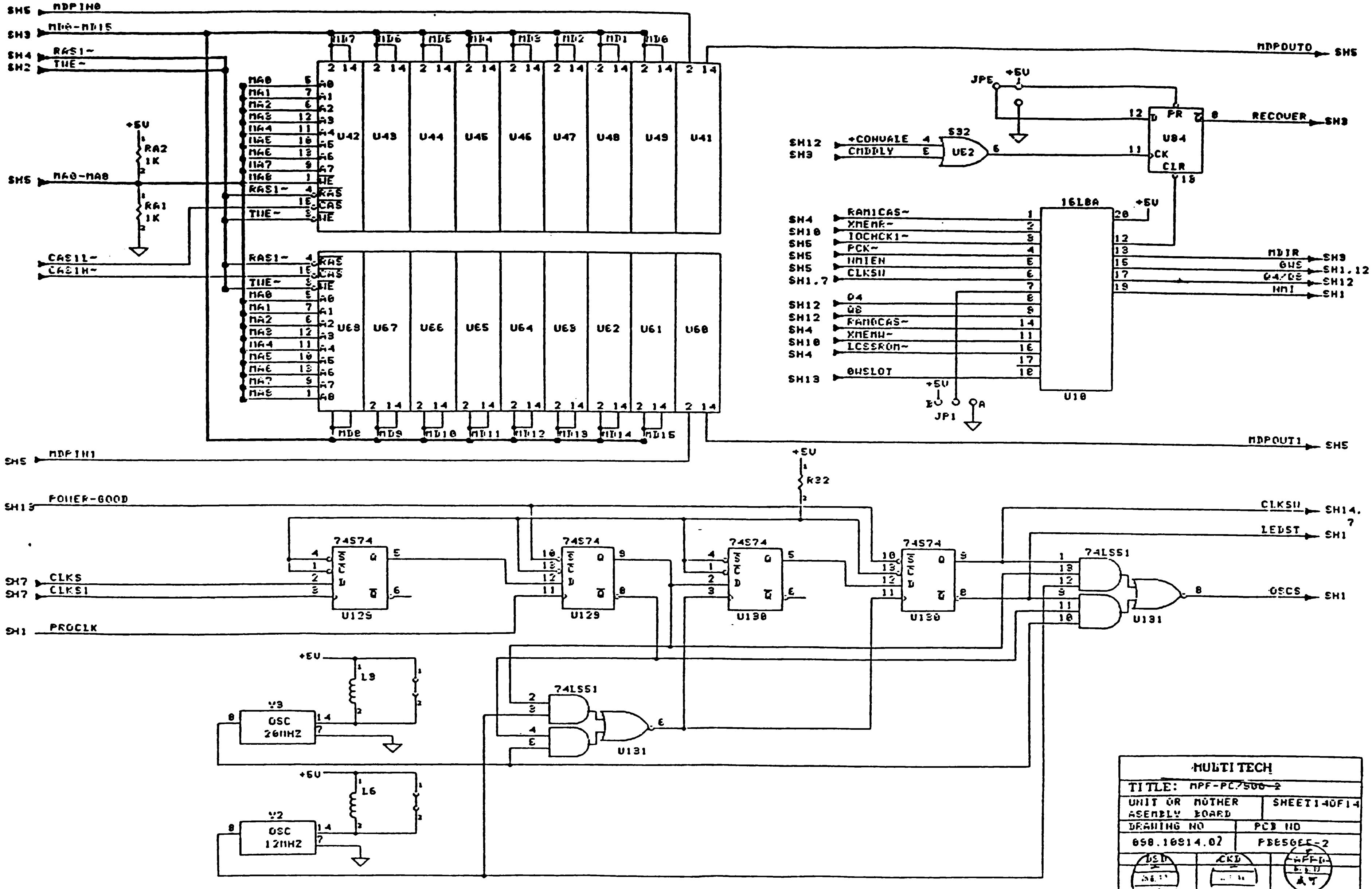

DMA MEMR~
SH10
8237A-5
U77
XA0-XA7
XD0-XD7
DRQ0
DRQ1
DRQ2
DRQ3
XIOR~
XIOW~
DMA MEMR~
XMEMW~
DMA 1 CS~
DMA RDY
DMA CLK
+RESET
HRQ
EOP
DACK0
DACK1
DCCK2
DACK3
DREQ0
DREQ1
DREQ2
DREQ3
IOR
IOW
MEMR
MEMW
CS
RDY
CLK
HLDA
RESET
PIN5
VCC
GND
ADSTB
AEN
+5V
RA6-4
10K
S00
U13
I/C
SH13
DACK0~
DACK1~
DACK2~
DACK3~
SH10,13
ALS573
U79
XA8
XA8-XA16
SH3
ALS00
U74
8237A-5
U76
HRQ1
SH9,6,10
+5V
RA6-5
10K
ALS573
U78
ALS10
U72
AEN2~
AEN1~
SH12
SH12,10
DRQ5
DRQ6
DRQ7
RESET
DMA2CS~
HLDA1
MASTER~
ALS04
U89
DACK4~
DACK5~
DACK6~
DACK7~
SH10
SH13
SH10,13
SH10,13
MULTITECH
TITLE: MPF-PC/900-2
UNIT OR MOTHER ASSEMBLY BOARD
DRAWING NO
098.10811.01
DSN
CKD



MULTI-TECH		
TITLE: MPF-PC/900-2		
UNIT OR MOTHER ASSEMBLY BOARD		SHEET 12 OF 14
DRAWING NO	PCB NO	
850.10812.01	PB85065-2	
DSD	CKD	APRD



MULTITECH	
TITLE: DPE-PC/900-2	
UNIT OR OTHER ASSEMBLY BOARD	SHEET 13 OF 14
DRAWING NO	PCB NO
898.10813.01	PB85865-2
DSD	CKD APPD



MDPIN0
MA0-MD15
RAS1~
THE~
MA0-MA8
CAS1L~
CAS1H~
MDPIN1
POWER-GOOD
CLKS
CLKS1
PROCLK
MDPOUT0
MDPOUT1
RECOVER
+CONVALE
CMDDLY
RAMICAS~
XMEMR~
IOCHCK1~
PCK~
NMIEN
CLKSN
Q4
Q8
RAM0CAS~
XMEMW~
LCSSROM~
0WSLOT
MDIR
GWS
Q4/Q8
NMI
16L8A
U18
U84
U82
U41
U42
U43
U44
U45
U46
U47
U48
U49
U60
U61
U62
U63
U64
U65
U66
U67
U68
74S74
U125
U129
U130
74LS51
U131
CLKSN
LEDST
OSCS
OSC 20MHZ
OSC 12MHZ
L5
L6
R32
RA1 1K
RA2 1K
JP1
JP5
+5V
SH1
SH2
SH3
SH4
SH5
SH7
SH10
SH12
SH13
SH14, 7
SH1, 12
SH1, 7
MULTITECH
TITLE: MPF-PC/500-2
UNIT OR ASSEMBLY MOTHER BOARD
SHEET 14 OF 14
DRAWING NO 058.10814.02
PCB NO PB8506E-2
DSN
CKD
APPD

S E R I A L / P A R A L L E L A D A P T E R

1 SERIAL PORT
1 PARALLEL PORT

AT/PC

I/O ADRESS-MAP SERIAL/PARALLEL ADAPTER

	0 1 2 3 4 5 6 7 I 8 9 A B C D E F	USED ON
270 H	X X X X X X X X I PARALLEL PORT 2	AT
280 H 290 H 2A0 H 2B0 H 2C0 H 2D0 H 2E0 H		
2F0 H	X X X X X X X X I SERIAL PORT 2	PC, AT
300 H 310 H 320 H 330 H 340 H 350 H 360 H		
370 H	X X X X X X X X I PARALLEL PORT 1	PC, AT
380 H 390 H 3A0 H		
3B0 H	MONOCHR.DISPLAY I PARALLEL PORT 0	PC, AT
3C0 H 3D0 H 3E0 H		
3F0 H	DISKETTE CONTR. I SERIAL PORT 1	PC, AT

INTERRUPTS SERIAL/PARALLEL ADAPTER

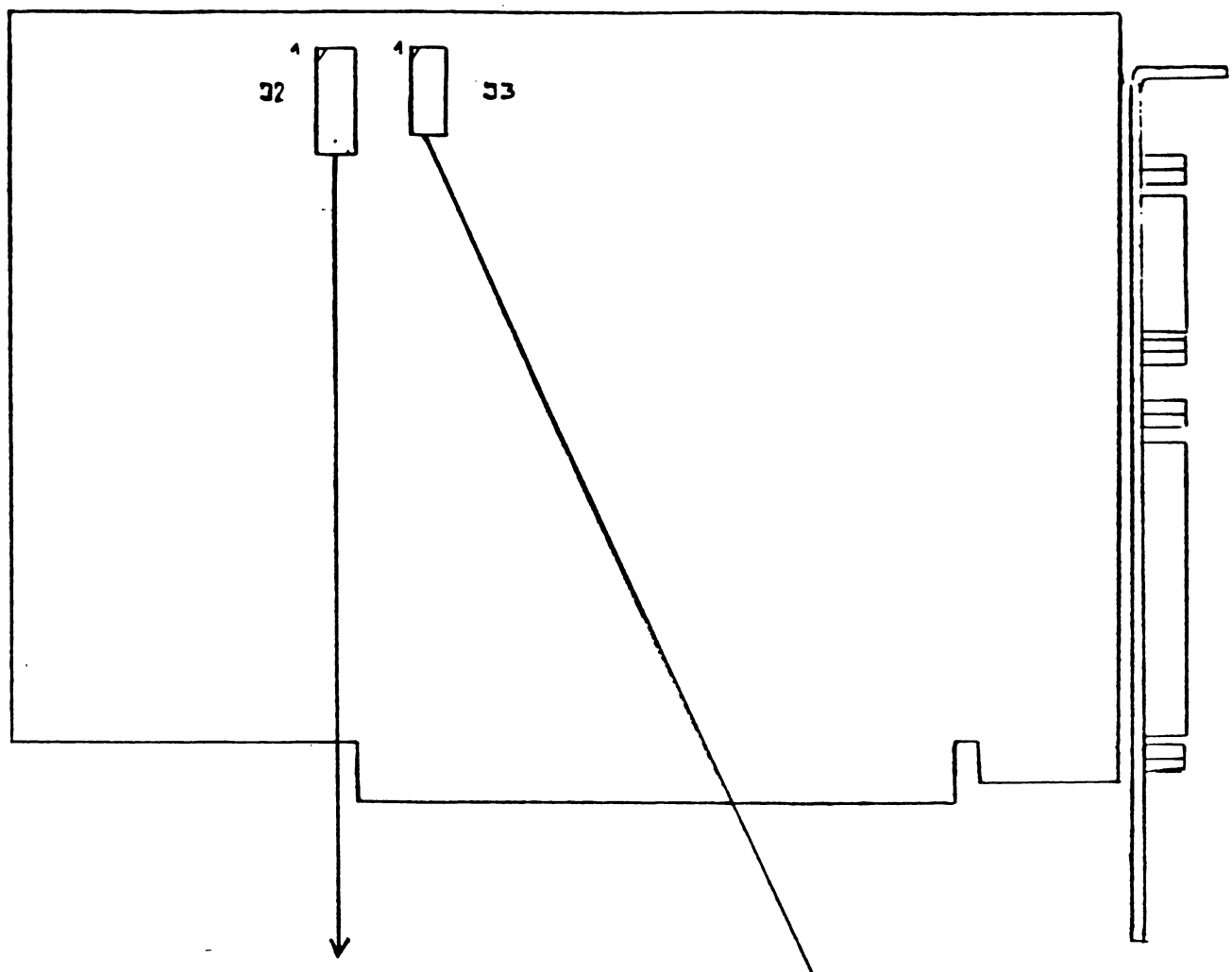
INTERRUPT	USED ON
IRQ 3	SERIAL PORT 2 (PC, AT)
IRQ 4	SERIAL PORT 1 (PC, AT)
IRQ 5	PARALLEL PORT 2 (AT)
IRQ 7	PARALLEL PORT 1 (PC, AT)
IRQ 7	PARALLEL PORT 0 (PC, AT)

I/O ADRESS PARALLEL 2, PARALLEL 1, PARALLEL 0

HEX	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	REGISTER SELECT		
278	1	0	0	1	1	1	1	0	0	0	DATA LATCH	R/W	PARALLEL 2
279	1	0	0	1	1	1	1	0	0	1	STATUS	R	
27A	1	0	0	1	1	1	1	0	1	0	CONTROL	R/W	
27B	1	0	0	1	1	1	1	0	1	1			
27C	1	0	0	1	1	1	1	1	0	0	DATA LATCH	R/W	
27D	1	0	0	1	1	1	1	1	0	1	STATUS	R	
27E	1	0	0	1	1	1	1	1	1	0	CONTROL	R/W	
27F	1	0	0	1	1	1	1	1	1	1			
378	1	1	0	1	1	1	1	0	0	0	DATA LATCH	R/W	PARALLEL 1
379	1	1	0	1	1	1	1	0	0	1	STATUS	R	
37A	1	1	0	1	1	1	1	0	1	0	CONTROL	R/W	
37B	1	1	0	1	1	1	1	0	1	1			
37C	1	1	0	1	1	1	1	1	0	0	DATA LATCH	R/W	
37D	1	1	0	1	1	1	1	1	0	1	STATUS	R	
37E	1	1	0	1	1	1	1	1	1	0	CONTROL	R/W	
37F	1	1	0	1	1	1	1	1	1	1			
3BC	1	1	1	0	1	1	1	1	0	0	DATA LATCH	R/W	PARALL 0
3BD	1	1	1	0	1	1	1	1	0	1	STATUS	R	
3BE	1	1	1	0	1	1	1	1	1	0	CONTROL	R/W	
3BF	1	1	1	0	1	1	1	1	1	1			

I/O ADRESS SERIAL 2, SERIAL 1

HEX	A9 A8	A7 A6 A5 A4	A3 A2 A1 A0	REGISTER SELECT	
2F8	1 0	1 1 1 1	1 0 0 0	TX/RX BUFF. R/W	S
2F9	1 0	1 1 1 1	1 0 0 1	INTR ENABLE REG.	E
2FA	1 0	1 1 1 1	1 0 1 0	INTR IDENT. REG.	R
2FB	1 0	1 1 1 1	1 0 1 1	LINE CONTR. REG.	I
2FC	1 0	1 1 1 1	1 1 0 0	MODEM CONTR.REG.	A
2FD	1 0	1 1 1 1	1 1 0 1	LINE STATUS REG.	L
2FE	1 0	1 1 1 1	1 1 1 0	MODEM STAT. REG.	2
21F	1 0	1 1 1 1	1 1 1 1	RESERVED	
3F8	1 1	1 1 1 1	1 0 0 0	TX/RX BUFF. R/W	S
3F9	1 1	1 1 1 1	1 0 0 1	INTR ENABLE REG.	E
3FA	1 1	1 1 1 1	1 0 1 0	INTR IDENT. REG.	R
3FB	1 1	1 1 1 1	1 0 1 1	LINE CONTR. REG	I
3FC	1 1	1 1 1 1	1 1 0 0	MODEM CONTR.REG.	A
3FD	1 1	1 1 1 1	1 1 0 1	LINE STATUS REG.	L
3FE	1 1	1 1 1 1	1 1 1 0	MODEM STAT. REG.	1
3FF	1 1	1 1 1 1	1 1 1 1	RESERVED	



PARALLEL 0 SELECT:

J 2

1	* *	2	
3	⟷	4	
5	⟷	6	
7	⟷	8	
9	* *	10	

PARALLEL 1 SELECT:

J 2

1	⟷	2	
3	* *	4	
5	⟷	6	
7	⟷	8	
9	* *	10	

PARALLEL 2 SELECT:

J 2

1	⟷	2	
3	⟷	4	
5	* *	6	
7	* *	8	
9	⟷	10	

Standard

SERIAL 1 SELECT:

J 3

1	⟷	2	
3	⟷	4	
5	* *	6	
7	* *	8	

SERIAL 2 SELECT:

J 3

1	* *	2	
3	* *	4	
5	⟷	6	
7	⟷	8	

Standard

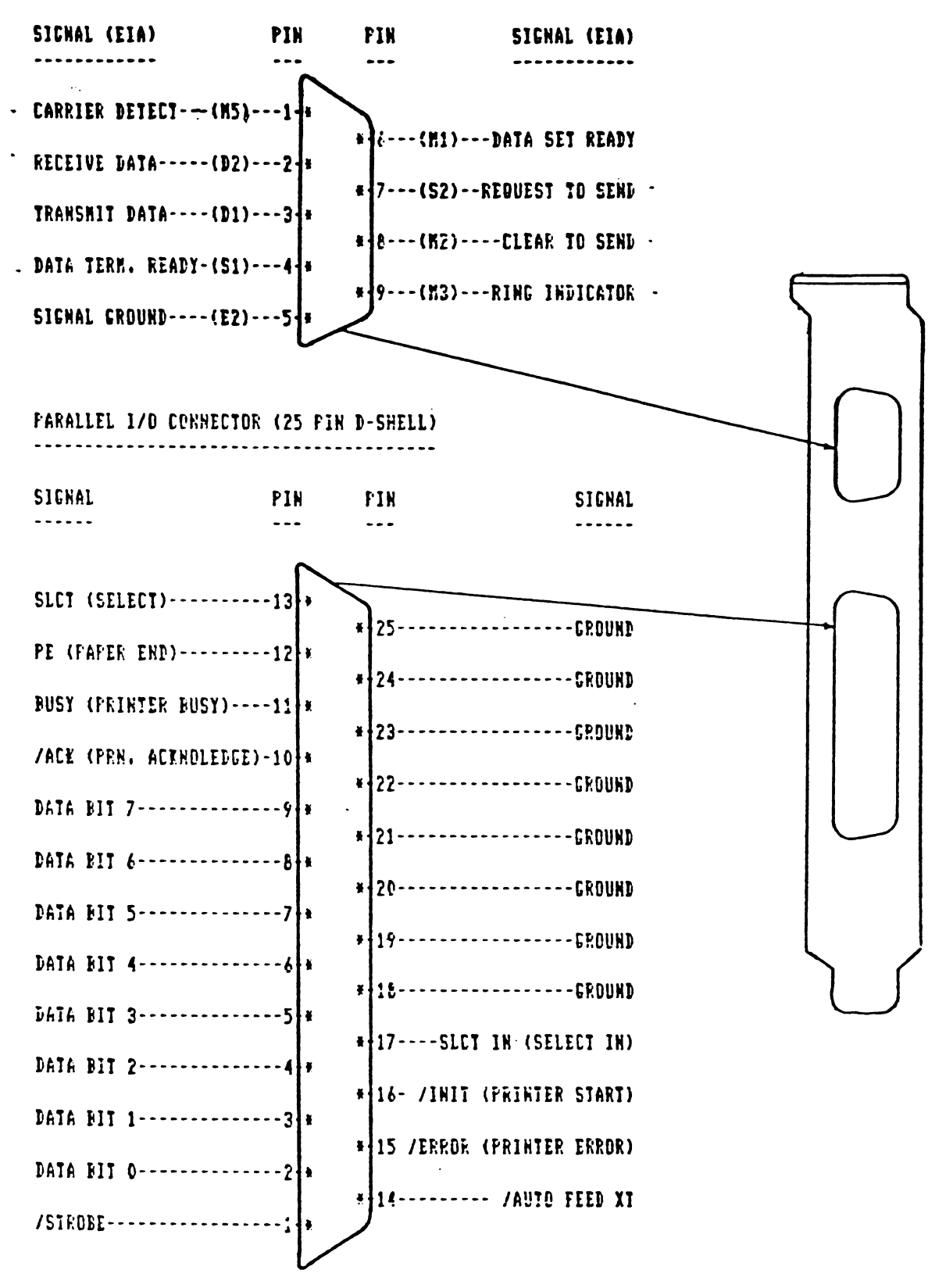
SERIAL/PARALLEL ADAPTER	DATE 23-11-1984	SHEET 5/10

CHARACTERISTICS OUTPUT DRIVER	
PARALLEL DATA, PROCESSOR IRQ	
SINK CURRENT	24.0 mA I MAX
SOURCE CURRENT	-2.6 mA I MAX
HIGH-LEVEL OUTPUT VOLTAGE	2.4 Vdc I MIN
LOW -LEVEL OUTPUT VOLTAGE	0.4 Vdc I MAX
PARALLEL CONTROL	
SINK CURRENT	16.0 mA I MAX
SOURCE CURRENT	0.55 mA I MAX
HIGH-LEVEL OUTPUT VOLTAGE	5.0 Vdc I -PU
LOW -LEVEL OUTPUT VOLTAGE	0.4 Vdc I MAX
PARALLEL PROCESSOR INTERFACE	
SINK CURRENT	24.0 mA I MAX
SOURCE CURRENT	-15.0 mA I MAX
HIGH-LEVEL OUTPUT VOLTAGE	2.0 Vdc I MIN
LOW -LEVEL OUTPUT VOLTAGE	0.5 Vdc I MAX

SERIAL INTERFACE		
ON SPACING CONDITION (BIN.0, POS.VOLTAGE)		
OFF MARKING CONDITION (BIN.1, NEG.VOLTAGE)		
ABOVE	+15 Vdc	INVALID
+ 3 Vdc TO +15 Vdc		ON
- 3 Vdc TO + 3 Vdc		INVALID
- 3 Vdc TO -15 Vdc		OFF
BELOW	-15 Vdc	INVALID

CONNECTORS ON EXTENSION SEAT PANEL

SERIAL I/O CONNECTOR (9 PIN D-SHELL)



DIAGNOSTIC WRAP PLUG PARALLEL I/O(25 PIN)

CONNECTIONS:

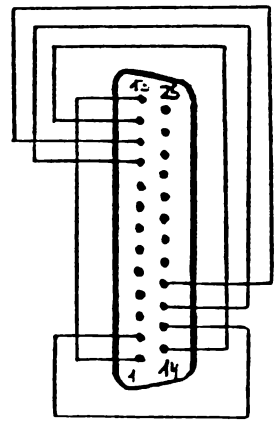
PIN 17	- PIN 11
/SLCT IN	- BUSY

PIN 16	- PIN 10
/INIT	- /ACK

PIN 15	- PIN 2
/ERROR	- DATA 0

PIN 14	- PIN 12
/AUTOFDXD	- PE

PIN 13	- PIN 1
SLCT	- /STROBE



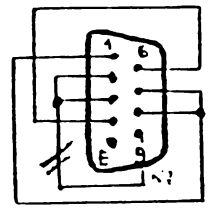
DIAGNOSTIC WRAP PLUG SERIAL I/O (9 PIN)

CONNECTIONS:

PIN 2	- PIN 3 - PIN 9
RXD(D2)	- TXD(D1) - RI(M3)

PIN 7	- PIN 8	- PIN 1
RTS(S2)	- CTS(M2)	- CD(M5)

PIN 6	- PIN 4
DSR(M1)	- DTR(S1)



Pin 9 abtrennen
10-03-86 Bo

DATE 03-19-1986

CBM - MACHINE - TYPE : PC AT, PC 10/20

DESIGNED BY : H.SCHMIDT

FPLA TYPE : N 82 S 100

LOCATION (BOARD/UNIT-NO) : SERIAL/PARALLEL ADAPTER/U 1

FUNKTION OF FPLA : I/O DECODER, READ/WRITE ACI, DIR TRANSCEIVER

REMARKS : ---

INPUT AND OUTPUT SIGNALS:

PIN NO.	IN-TERM	NAME
20	15	SEL P1
21	14	SEL P2
22	13	SEL S1
23	12	/IOR
24	11	/IOW
25	10	AEN
26	9	A9
27	8	A8
2	7	A7
3	6	A6
4	5	A5
5	4	A4
6	3	A3
7	2	A2
8	1	A1
9	0	A0

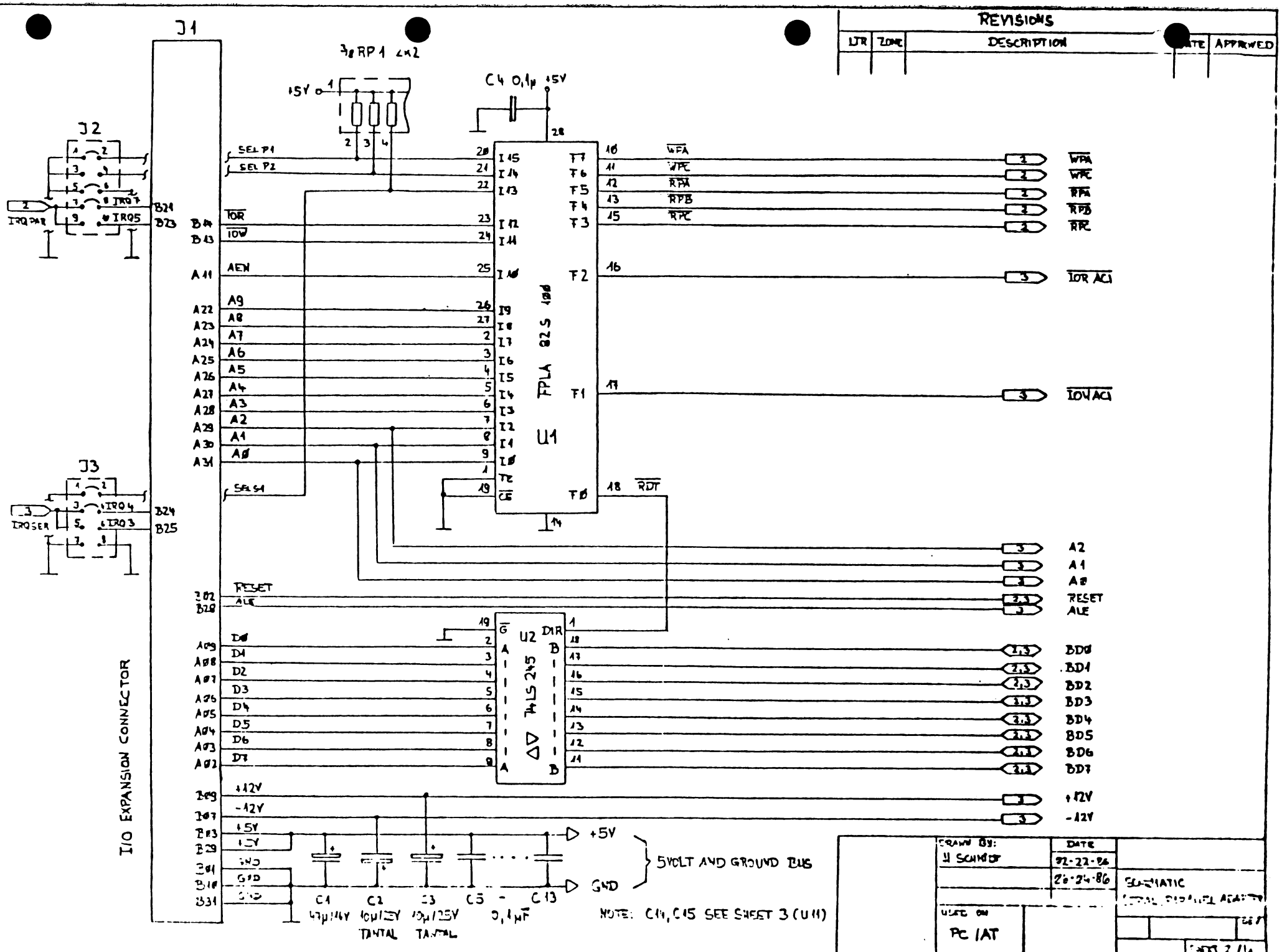
PIN NO.	OUT	NAME
10	7	/WPA
11	6	/WPC
12	5	/RPA
13	4	/RPB
15	3	/RPC
16	2	/IOR ACI
17	1	/IOW ACI
18	0	/RDI
1	FE	GND
14	GND	GND
19	/CE	GND
28	VCC	+5V

```
*A LLLLLLLL                                          ;ACTIVE OUTPUT LEVELS
*P 00  *I --LLHLHHHHHHH--- *F .....A.A ;READ COM 1
*P 01  *I --HLHLHLHHHHH--- *F .....A.A ;READ COM 2
*P 02  *I HL-LHLHHHLHHHHHL *F ....A..A ;READ PAR.0 CONTROL
*P 03  *I LH-LHLHHLHHHH-HL *F ....A..A ;READ PAR.1 CONTROL
*P 04  *I LL-LHLHLLHHHH-HL *F ....A..A ;READ PAR.2 CONTROL
*P 05  *I HL-LHLHHHLHHHHLH *F ...A...A ;READ PAR.0 STATUS
*P 06  *I LH-LHLHHLHHHH-LH *F ...A...A ;READ PAR.1 STATUS
*P 07  *I LL-LHLHLLHHHH-LH *F ...A...A ;READ PAR.2 STATUS
*P 08  *I HL-LHLHHHLHHHHLL *F ..A....A ;READ PAR.0 DATA
*P 09  *I LH-LHLHHLHHHH-LL *F ..A....A ;READ PAR.1 DATA
*P 10  *I LL-LHLHLLHHHH-LL *F ..A....A ;READ PAR.2 DATA
*P 11  *I --LHLLHHHHHHH--- *F ......A. ;WRITE COM 1
*P 12  *I --HHLLHLHHHHH--- *F ......A. ;WRITE COM 2
*P 13  *I HL-HLLHHHLHHHHHL *F .A...... ;WRITE PAR.0 CONTROL
*P 14  *I LH-HLLHHLHHHH-HL *F .A...... ;WRITE PAR.1 CONTROL
*P 15  *I LL-HLLHLLHHHH-HL *F .A...... ;WRITE PAR.2 CONTROL
*P 16  *I HL-HLLHHHLHHHHLL *F A....... ;WRITE PAR.0 DATA
*P 17  *I LH-HLLHHLHHHH-LL *F A....... ;WRITE PAR.1 DATA
*P 18  *I LL-HLLHLLHHHH-LL *F A....... ;WRITE PAR.2 DATA
*P 19  *I 0000000000000000 *F AAAAAAAA ;
*P 20  *I 0000000000000000 *F AAAAAAAA ;
*P 21  *I 0000000000000000 *F AAAAAAAA ;
*P 22  *I 0000000000000000 *F AAAAAAAA ;
*P 23  *I 0000000000000000 *F AAAAAAAA ;
*P 24  *I 0000000000000000 *F AAAAAAAA ;
*P 25  *I 0000000000000000 *F AAAAAAAA ;
*P 26  *I 0000000000000000 *F AAAAAAAA ;
*P 27  *I 0000000000000000 *F AAAAAAAA ;
*P 28  *I 0000000000000000 *F AAAAAAAA ;
*P 29  *I 0000000000000000 *F AAAAAAAA ;
*P 30  *I 0000000000000000 *F AAAAAAAA ;
*P 31  *I 0000000000000000 *F AAAAAAAA ;
*P 32  *I 0000000000000000 *F AAAAAAAA ;
*P 33  *I 0000000000000000 *F AAAAAAAA ;
*P 34  *I 0000000000000000 *F AAAAAAAA ;
*P 35  *I 0000000000000000 *F AAAAAAAA ;
*P 36  *I 0000000000000000 *F AAAAAAAA ;
*P 37  *I 0000000000000000 *F AAAAAAAA ;
*P 38  *I 0000000000000000 *F AAAAAAAA ;
*P 39  *I 0000000000000000 *F AAAAAAAA ;
*P 40  *I 0000000000000000 *F AAAAAAAA ;
*P 41  *I 0000000000000000 *F AAAAAAAA ;
*P 42  *I 0000000000000000 *F AAAAAAAA ;
*P 43  *I 0000000000000000 *F AAAAAAAA ;
*P 44  *I 0000000000000000 *F AAAAAAAA ;
*P 45  *I 0000000000000000 *F AAAAAAAA ;
*P 46  *I 0000000000000000 *F AAAAAAAA ;
*P 47  *I 0000000000000000 *F AAAAAAAA ;
```

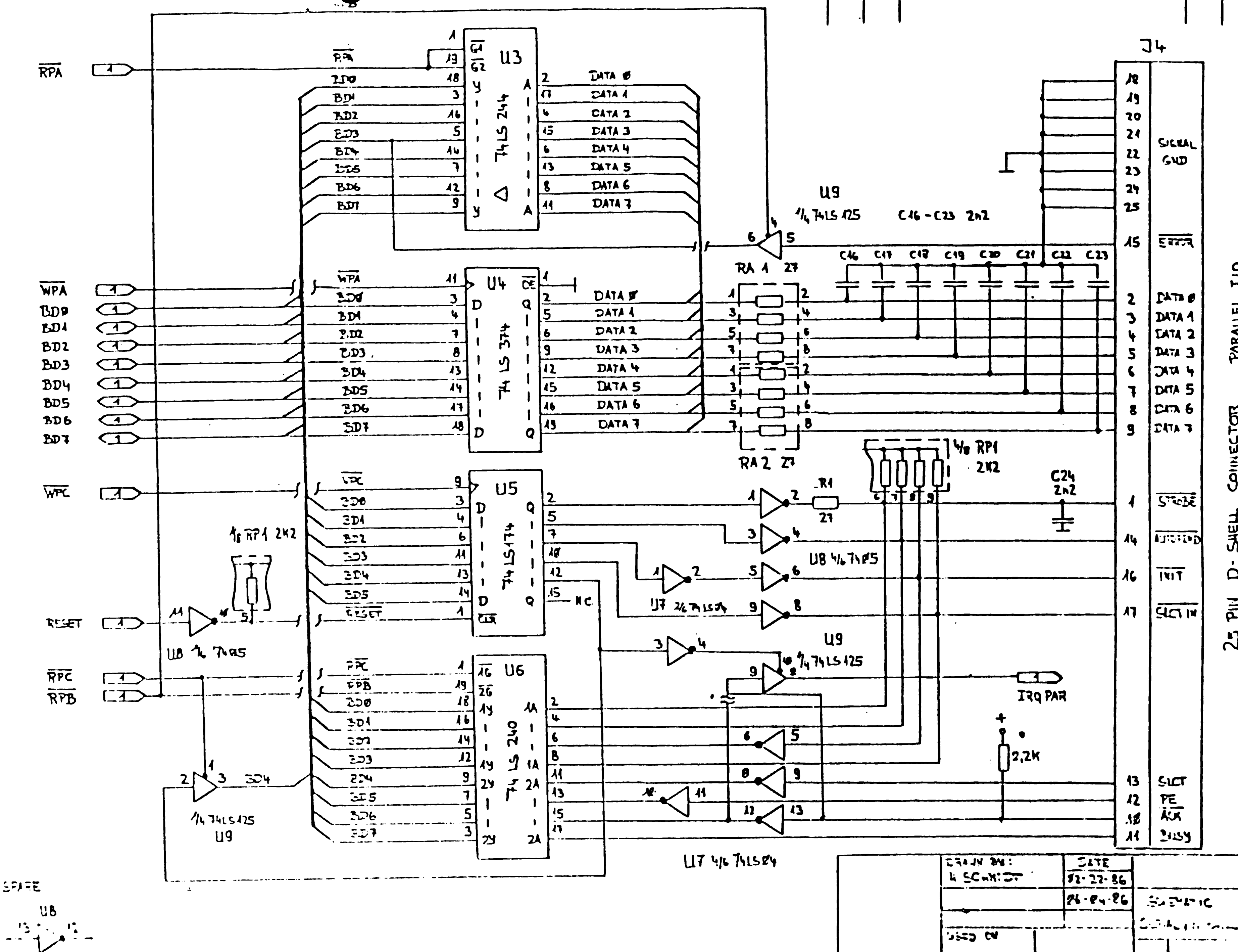
SERIAL / PARALLEL ADAPTER

1 SERIAL PORT
1 PARALLEL PORT

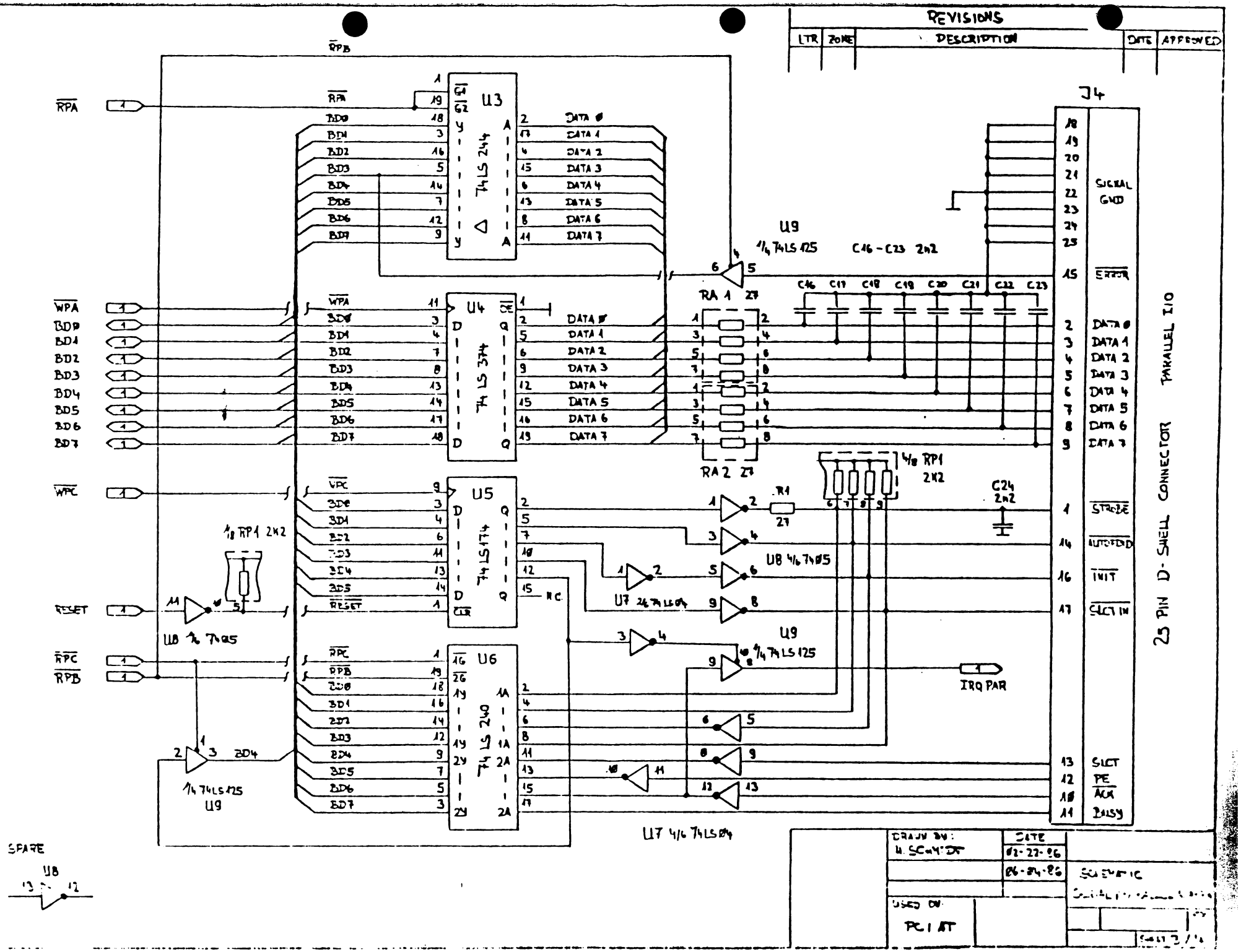
AT/PC

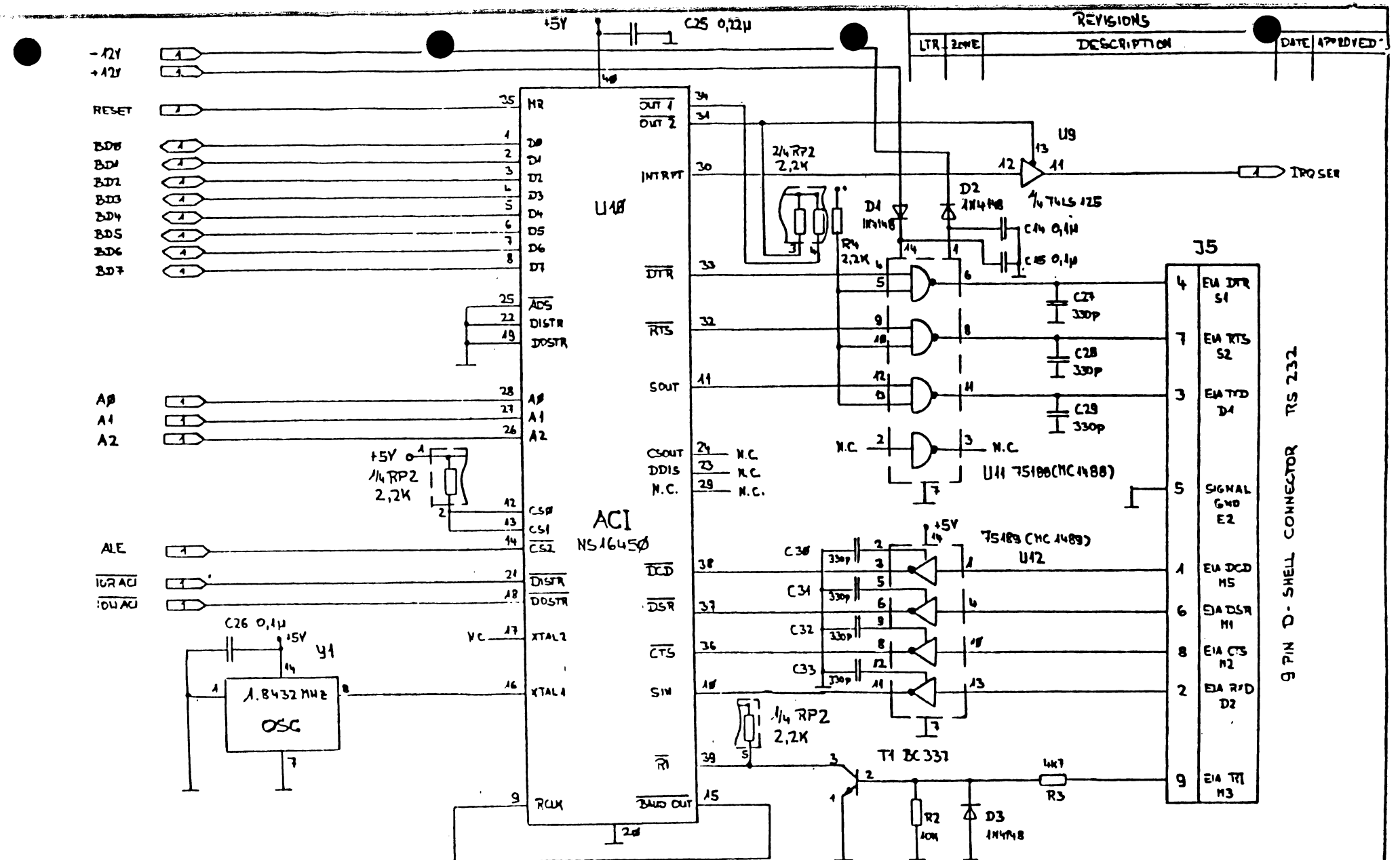

REVISIONS
LTR
ZONE
DESCRIPTION
DATE
APPROVED
J1
J2
J3
RP1 4x2
+5V
C4 0,1µ
U1
FPLA 82S 100
U2
74LS245
SEL P1
SEL P2
SEL S1
IOR
IOW
AEN
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
RESET
ALE
D0
D1
D2
D3
D4
D5
D6
D7
WFA
WFC
RFA
RFB
RFC
IOR ACT
IOW ACT
RDT
+12V
-12V
GND
IRQ2
IRQ3
IRQ4
IRQ5
IRQSEL
I/O EXPANSION CONNECTOR
C1 47µ/16V TANTAL
C2 10µ/25V TANTAL
C3 10µ/25V TANTAL
C5 - C13 0,1µF
+5V
GND
5VOLT AND GROUND BUS
NOTE: C14, C15 SEE SHEET 3 (U11)
DRAWN BY: U SCHMIDT
DATE 12-22-86
26-24-86
USED ON PC/AT
SCHEMATIC
SHEET 2/14

LTR	ZONE	REVISIONS DESCRIPTION	DATE	APPROVED



DRAWN BY:	DATE	
L SCHMIDT	02-22-86	
	26-04-86	SCHEMATIC
USED ON PC I AT		


REVISIONS
LTR
ZONE
DESCRIPTION
DATE
APPROVED
RPB
RPA
WPA
WPC
RPC
RESET
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
U3
74LS 244
U4
74 LS 374
U5
74LS174
U6
74 LS 240
U9
1/4 74LS125
C46 - C23 2n2
RA 1 Z9
RA 2 Z9
4/8 RP1 2K2
1/8 RP1 2K2
R1
Z9
C24
2n2
U8 4/6 74LS05
U7 2/6 74LS08
U7 4/6 74LS08
IRQ PAR
J4
SIGNAL GND
ERROR
STROBE
AUTOFEED
INIT
SLCT IN
SLCT
PE
ACK
BUSY
25 PIN D-SHELL CONNECTOR PARALLEL I/O
SPARE
U8
DRAWN BY:
H. SCHMIDT
DATE
02-22-86
06-24-86
SCHEMATIC
USED ON
PC / AT


REVISIONS
LTR
ZONE
DESCRIPTION
DATE
APPROVED
-12V
+12V
RESET
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
A0
A1
A2
ALE
IOR ACI
IOW ACI
+5V
C25 0,22µ
U18
ACI
NS16450
MR
D0
D1
D2
D3
D4
D5
D6
D7
ADS
DISTR
DOSTR
CS0
CS1
CS2
XTAL2
XTAL1
RCLK
OUT 1
OUT 2
INTRPT
DTR
RTS
SOUT
CSOUT
DDIS
N.C.
DCD
DSR
CTS
SIN
RI
BAUD OUT
2/4 RP2 2,2K
1/4 RP2 2,2K
D1 1N4148
D2 1N4148
R4 2,2K
U9
1/4 74LS 125
IRQ SER
C24 0,1µ
C25 0,1µ
C27 330p
C28 330p
C29 330p
U11 75188(MC1488)
C30 330p
C31 330p
C32 330p
C33 330p
U12 75189 (MC 1489)
C26 0,1µ
Y1
1.8432 MHz
OSC
T1 BC 337
4K7
R3
R2 10K
D3 1N4148
J5
9 PIN D-SHELL CONNECTOR RS 232
EIA DTR S1
EIA RTS S2
EIA TXD D1
SIGNAL GND E2
EIA DCD M5
EIA DSR M1
EIA CTS M2
EIA RXD D2
EIA RI M3
DRAWN BY: H. SCHMIDT
DATE 22.12.86
06.8.86
SCHEMATIC
USED ON PC/AT.

RW Elektro-Elektronik GmbH

Model No: RW - SNT 220/001

RW Elektro-Elektronik GmbH

Peiner Str. 237, 3320 Salzgitter 1 / West-Germany

Telex : 9 54 534 cgmrw
Telefon : 0 53 41 / 6 14 44-45
Fax : 0 53 41 / 6 14 44

S p e c i f i c a t i o n

1. Generalities

1.1 Efficiency	(full load)	70 % type
1.2 MTBF	35° C ambient air, nominal line, all outputs at 75 % load	50 000 hrs min
1.3 Operating Temperature	(full output power)	0 - 60° C
1.4 Storage Temperature		- 40° ... + 70° C
1.5 Hold-up Time	(minmum input 180 VAC, all outputs 75 % load)	10 msec min
1.6 EMI Filter	An internal EMI filter is required at the input of the power supply	

2. Input

2.1 AC nominal Input Voltage	230 V AC
2.1 AC Input Voltage range	180 - 270 V AC
2.2 AC Input Frequency	50 - 60 Hz
2.3 Input Surge Protection	3 KV, 25 A for 35 µs
2.4 Maximum of Inrush current	100 A

3. Output

3.1 Continous Output Power:

a) + 5 V / 3,0 - 20,0 A
b) + 12 V / 0,0 - 8,0 A
c) - 12 v / 0,0 - 0,3 A
d) - 5 V / 0,0 - 0,3 A

3.2 Regulation: (Note 3)

a) + 5 V - 4% / +%5%
b) + 12 V - 4% / + 5%
c) - 12 V +/ - 5%
d) - 5 V +/ - 5%

3.3 Ripple & Noise: (Note 3)

a) + 5 V 50 mVpp max
b) + 12 V 100 mVpp max
c) - 12 V 100 mVpp max
d) - 5 V 100 mVpp max

3.4 + 5 V DC Range: +/- 5%

3.5 + 5 V DC Initial Setting +/- 1%

(at nominal input voltage with:
a) + 5 V , 3,0 A
b) + 12 V , 0,0 A
c) - 12 V , 0,0 A
d) - 5 V , 0,0 A

3.6 Overvoltage Protection: (Note 4)

a) + 5 V : 6.0 VDC max
b) + 12 V : + 12 V + 15 %

3.7 Overcurrent Protection:

The unit withstands a short circuit (100 milliohm) condition on any or all outputs for an indefinite duration without demage.

3.8 Transient Response at all outputs: +/- 2%

(in following test condition:
a) + 5 V , 5.0 A
b) + 12 V , I = 1.0 A)

3.9 Power-good Signal: (Note 5)

The unit generates a power good signal, which indicates, that all power outputs are settled.

4. Notes

4.1 Total regulation is defined as the total maximum plus or minus percent deviation of the power supply from the specified nominal output level caused by any combination of variations of the following parameters over theirs specified ranges:

AC Input Voltage
Cross Regulation
Load Regulation
Temperature
Ripply & Noise

4.2 Cross and load regulation are defined for the load ranges, defined in § 3.1.

4.3 Ripple & noise is measured at full rated load and is the peak to peak combining both the ripple and noise levels of each output.
(Measurement to be made directly at the output connector.)

4.4 In overvoltage protection, all outputs must be protected but not necessarly individually. Overvoltage an any output will cause a latched shutdown of the entire supply.

4.5 The power good signal is an open collector output, which is TTL compatible and able to sink 3.2 mA.

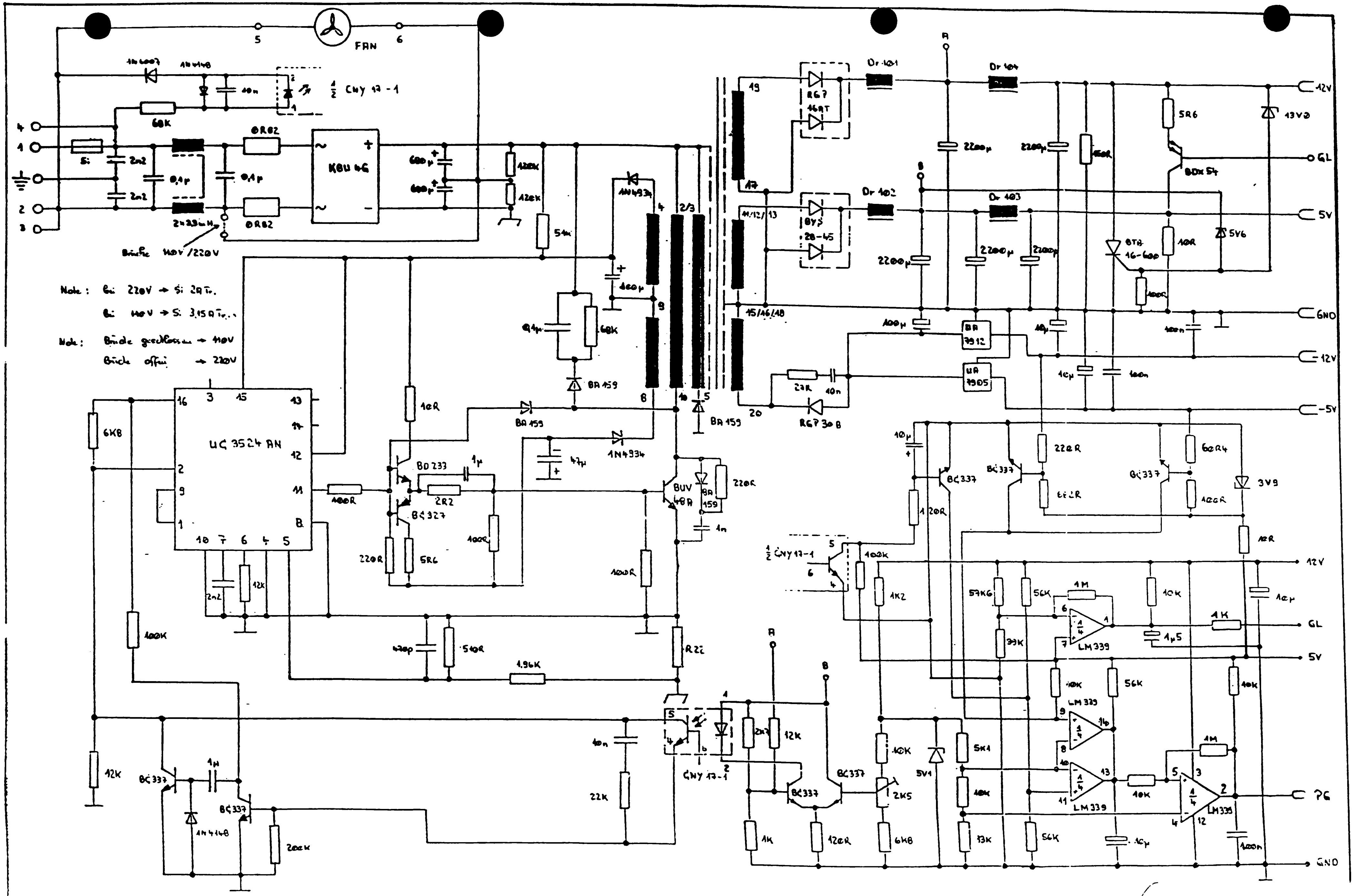
The power good signal goes high when the + 5 V , + 12 V , - 5 V output are above the minimum level (shown in the table below) and has a turn-on delay of 500 ms.

Output	Sense level
+ 5 V	+ 4.5 V
+ 12 V	+ 10.8 V
- 12 V	- 10.4 V
- 5 V	- 3.75 V

Conn.	Pin	Size AWG	Wire Colour	Voltage or Use	Unit	Cable Length (mm)
CN 1	1	18	Brown	Pwr good	CPU	220
	2	18	Yellow	+ 5 V		
	3	18	Orange	+ 12 V		
	4	18	Red	- 12 V		
	5	18	Blue	GND		
	6	18	Blue	GND		
CN 2	1	18	Blue	GND	CPU	220
	2	18	Blue	GND		
	3	18	Green	- 5 V		
	4	18	Yellow	+ 5 V		
	5	18	Yellow	+ 5 V		
	6	18	Yellow	+ 5 V		
CN 3/4	1	18	Orange	+ 12 V	Floppy #1	330/170
	2	18	Blue	GND		
	3	18	Blue	GND		
	4	18	Yellow	+ 5 V		
CN 5/6	1	18	Orange	+ 12 V	Floppy #2	330/170
	2	18	Blue	GND		
	3	18	Blue	GND		
	4	18	Yellow	+ 5 V		

5.2 Connector Schedule

Conn.	Vendor	Housing	Pin	Notes
CN 1/2	Burndy	GTC 6P-1	PCK 18-2TR9	
CN 3/4/5/6	J.S.T.	LCP-04	SLC-21T-2.0	



Benennung: RW - SNT 220/001

Gez.:

Rev.: R01

1

Multitech HARDDISK Configuration 16.09.1986
****

1) Systemabhaengige (BIOS) aktuelle Adresse fuer Harddisktyp

```
                          LO HI LO HI
0000:0100  05 EC 00 F0 11 E4 00 F0 - 7E 83 00 F0 7E 83 00 FF
                          SegLO SegHI
```

2) Tabelle im BIOS

	CY LO	CY HI	HE			PC LO	PC HI		CB					PZ LO	PZ HI	ST	
F000:E400	00	32	01	04	00	00	80	00	-	00	00	00	00	00	31	01	11	Type 1
F000:E410	00	67	02	04	00	00	2C	01	-	00	00	00	00	00	67	02	11	Type 2
F000:E420	00	67	02	06	00	00	2C	01	-	00	00	00	00	00	67	02	11	Type 3
F000:E430	00	AC	03	08	00	00	00	02	-	00	00	00	00	00	AC	03	11	Type 4
F000:E440	00	AC	03	06	00	00	00	02	-	00	00	00	00	00	AC	03	11	Type 5
F000:E450	00	67	02	04	00	00	FF	FF	-	00	00	00	00	00	67	02	11	Type 6
F000:E460	00	CE	01	08	00	00	00	01	-	00	00	00	00	00	FF	01	11	Type 7
F000:E470	00	DD	02	05	00	00	2C	01	-	00	00	00	00	00	DD	02	11	Type 8
F000:E480	00	84	03	0F	00	00	FF	FF	-	00	08	00	00	00	85	03	11	Type 9
F000:E490	00	34	03	03	00	00	FF	FF	-	00	00	00	00	00	34	03	11	Type 10
F000:E4A0	00	57	03	05	00	00	FF	FF	-	00	00	00	00	00	57	03	11	Type 11
F000:E4B0	00	57	03	07	00	00	FF	FF	-	00	00	00	00	00	57	03	11	Type 12
F000:E4C0	00	32	01	08	00	00	80	00	-	00	00	00	00	00	3F	01	11	Type 13
F000:E4D0	00	DD	02	07	00	00	FF	FF	-	00	00	00	00	00	DD	02	11	Type 14
F000:E4E0	00	D1	03	05	00	00	2C	01	-	00	00	00	00	00	D1	03	11	Type 15
F000:E4F0	00	FF	FF	FF	FF	FF	FF	FF	-	FF	FF	FF	FF	FF	FF	FF	FF	Type 16

ab Type 16 aufwaerts immer FF

CY = Anzahl der Zylinder
PC = Precompensation
PZ = Park-Zone
HE = Anzahl der Koepfe
CB = Control Byte (mehr als 8 Koepfe)
ST = Anzahl der Sektoren pro Track

Type	Zylinder	Koepfe
1	306	4
2	615	4
3	615	6
4	940	8
5	940	6
6	615	4
7	462	8
8	733	5
9	900	15
10	820	3
11	855	5
12	855	7
13	306	8
14	733	7
15	977	5

Tandon TM262 Type 6
NEC D5126 Type 2

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